D R A F T for comments
not for distribution

Scalable Readout System

from test systems to very large LHC systems
proposal for RD51

based on existing concepts:

Data and Trigger streams via GBE (LHCb)
DATE readout software (ALICE DAQ)
DCS: networked Linux mezzanine card with TTC chip (ALICE/ KIP Heidelberg)
HV bias control on FEE (ALICE PHOS)
High bandwidth LVDS data transfer via Network cables (ALICE EMCal)
LCU board (ALICE EMCal, under design)

Motivation

- Readout system for gas, pixel and photo detectors
- Plug-in frontend interface for application specific ASICS
- Scalable from test system to very large readout system
- User friendly and proven data acquisition system DATE for offline data analysis and presentation in Root
- Gigabit standard via copper or fiber between readout electronics and computers
- Control and data bidirectional over same links
- Standard coax I/O for trigger and clock distribution
- TTC option for optical LHC clock and control distribution
- hierarchical architecture based on 2 general purpose link adapters: SRU's and FEEs

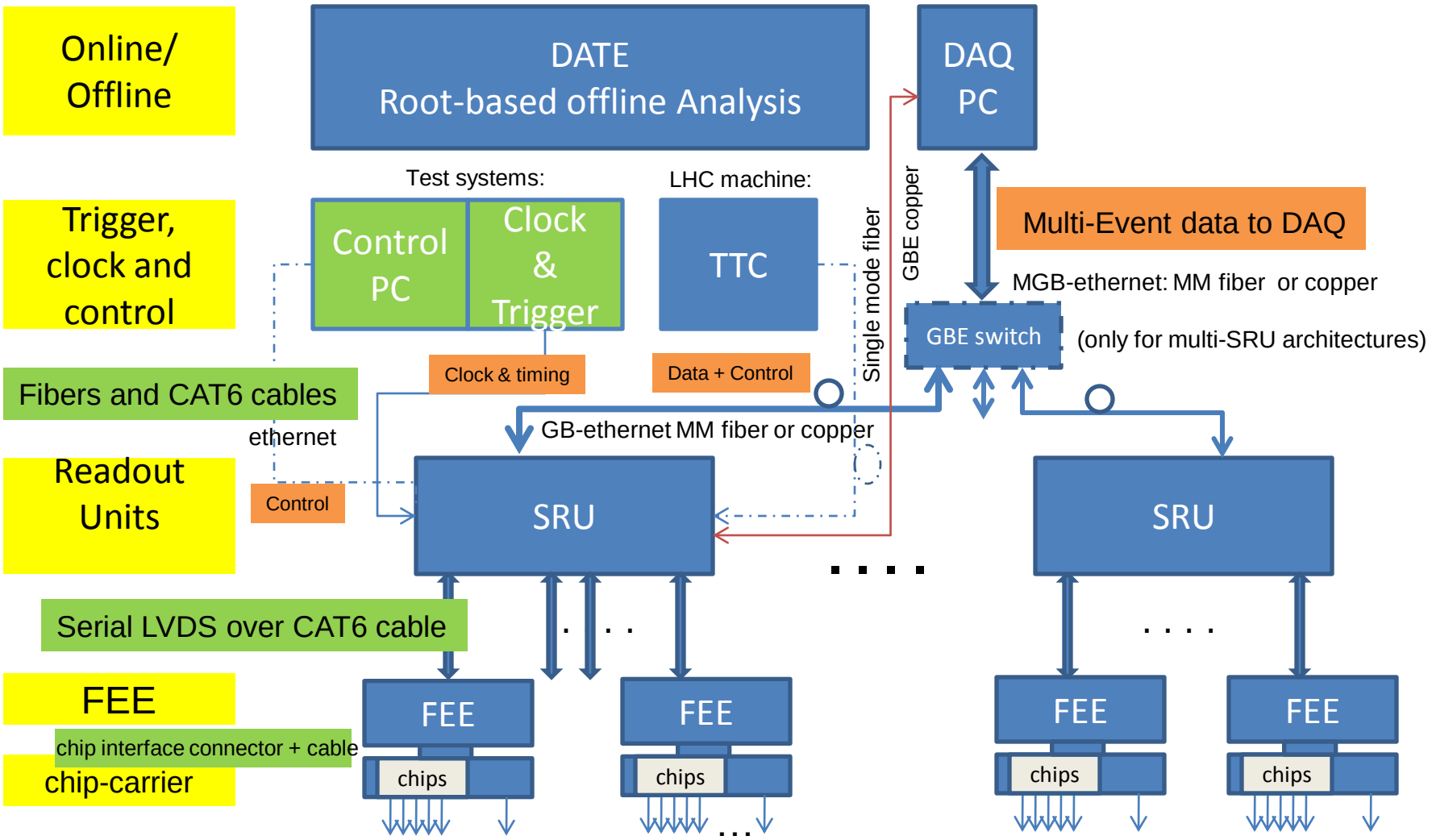
People, Teams*

- Dr. H. Muller, CERN PH: scalable RO proposal to RD51
- Dr. H. Taureg, CERN PT, RD51 secretary: coordination
- Dr. W. Riegler, CERN PH: RD51 convenor WG on Electronics & Readout systems
- Dr. H. Hillemanns, CERN DG/KTT Technology Transfer officer
- Dr. J. Wotschak, CERN PH, for ATLAS MMega project: test-systems with Altro and After chip frontend
- Dr. P. van de Vyvre, CERN PH, for ALICE DATE support, new Gigabit ethernet port
- Dr. Jose Toledo , Univ. o. Valencia: electronics for PET scanners

  + A.Tarazona , student of Univ. o Valencia, NEXT project: Gigabit Eth. firmware
- Rui Pimenta, Satellite services: LCU and FEE electronics design
- Dr. Alex Walsch, GE Global Research, Garching Munich: research application
- Dr. Yaping Wang, CCNU Wuhan: Offline standard Root-based analysis
- NN, NN : Board controller firmware, User Interface, Chip carrier design

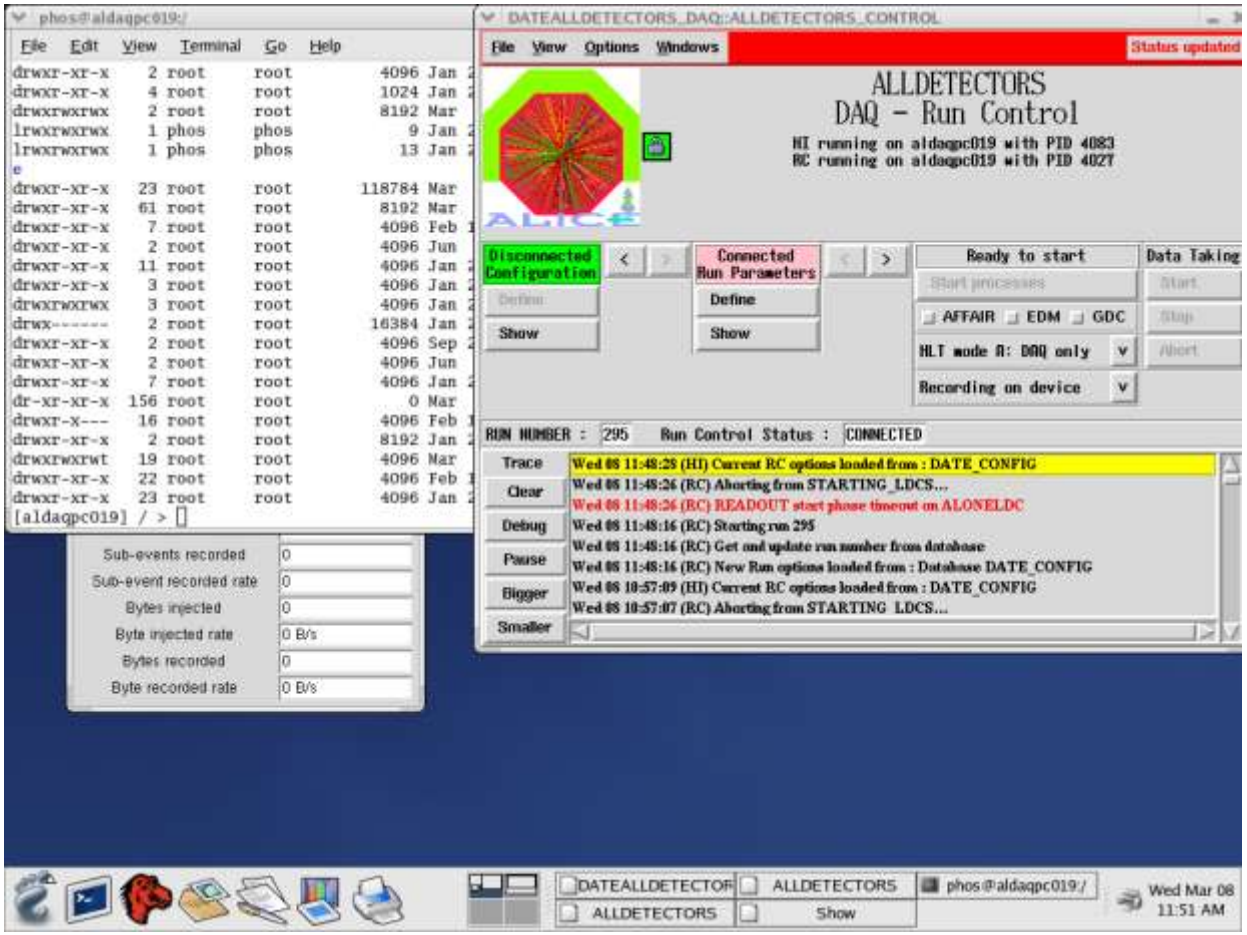
* to be confirmed

Scalable concept in a nutshell



DATE Data Acquisition software

http://ph-dep-aid.web.cern.ch/ph-dep-aid/



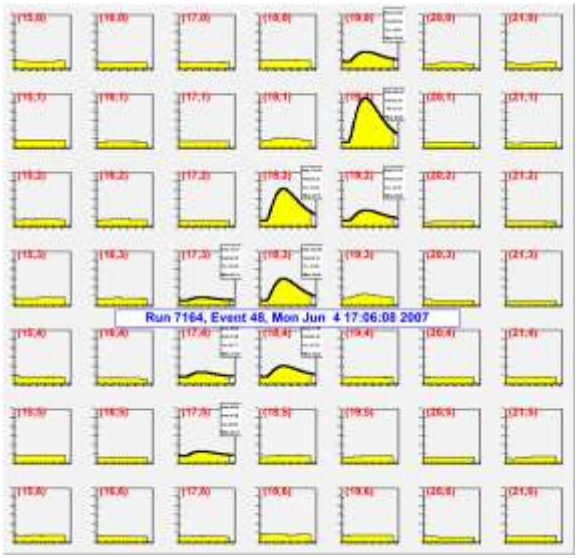
-Linux-based
-baseline for all
ALICE detectors
-also used
by other users
-easy User interface
-very well documented
-in use both for test-
systems and full
ALICE detector system
-root file storage
-I/O interface to
MM fiber
-porting to GBE over MM
fiber started

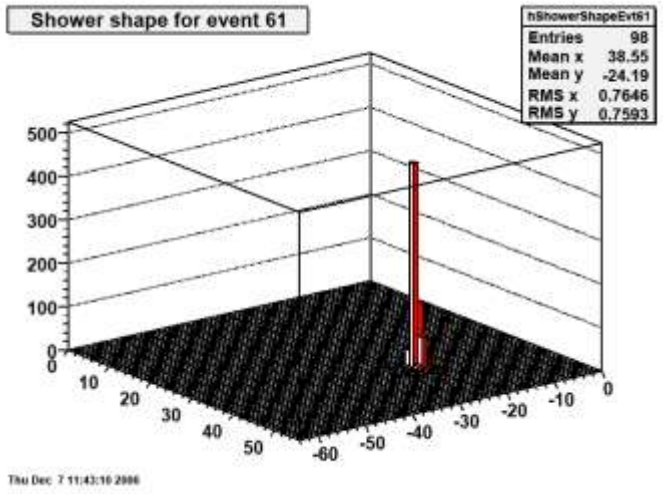
Root Data Analysis

http://root.cern.ch/

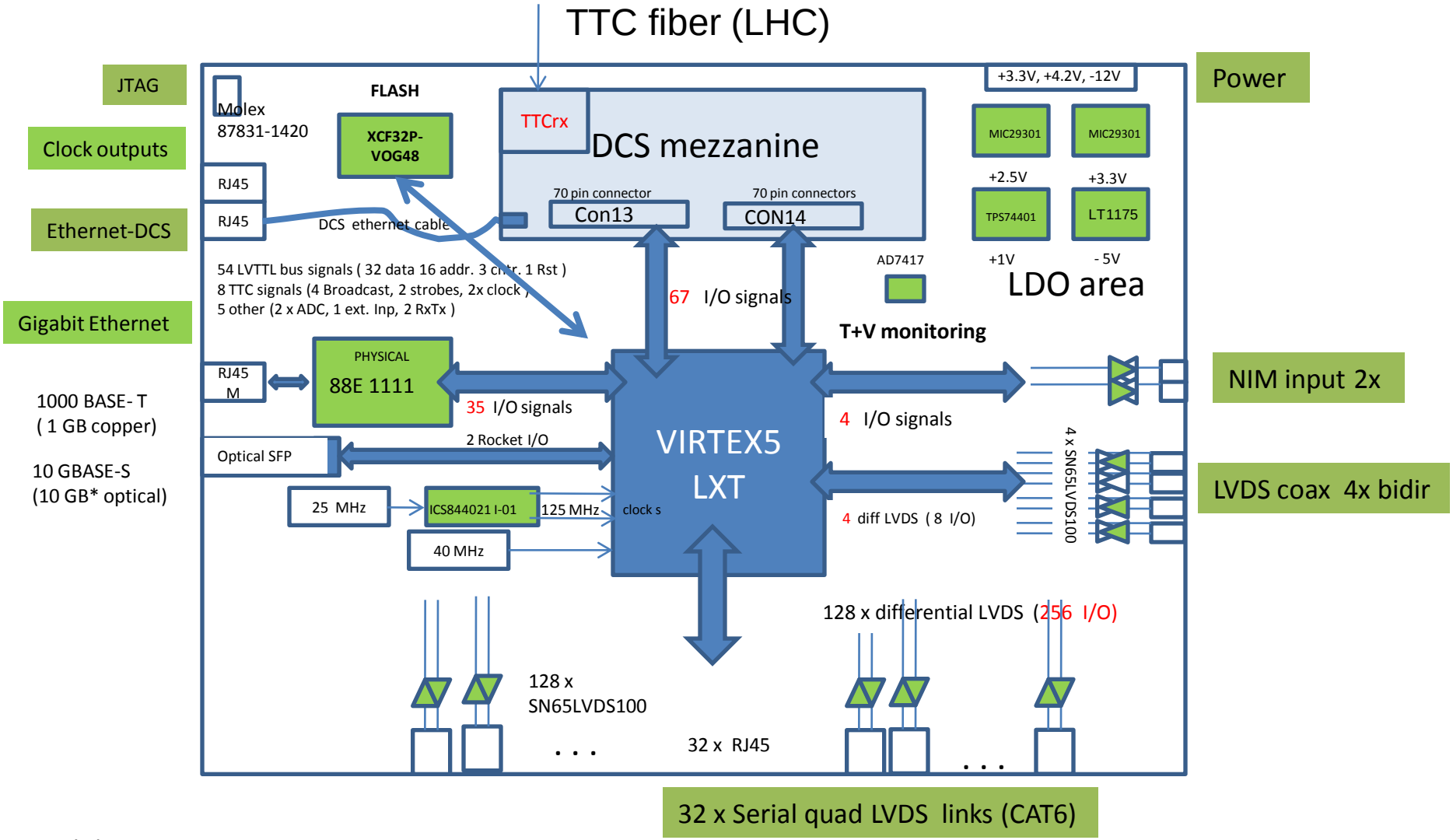
Baseline Data Analysis Package for LHC experiments

Example of Root analysis with a simple 1PC test system



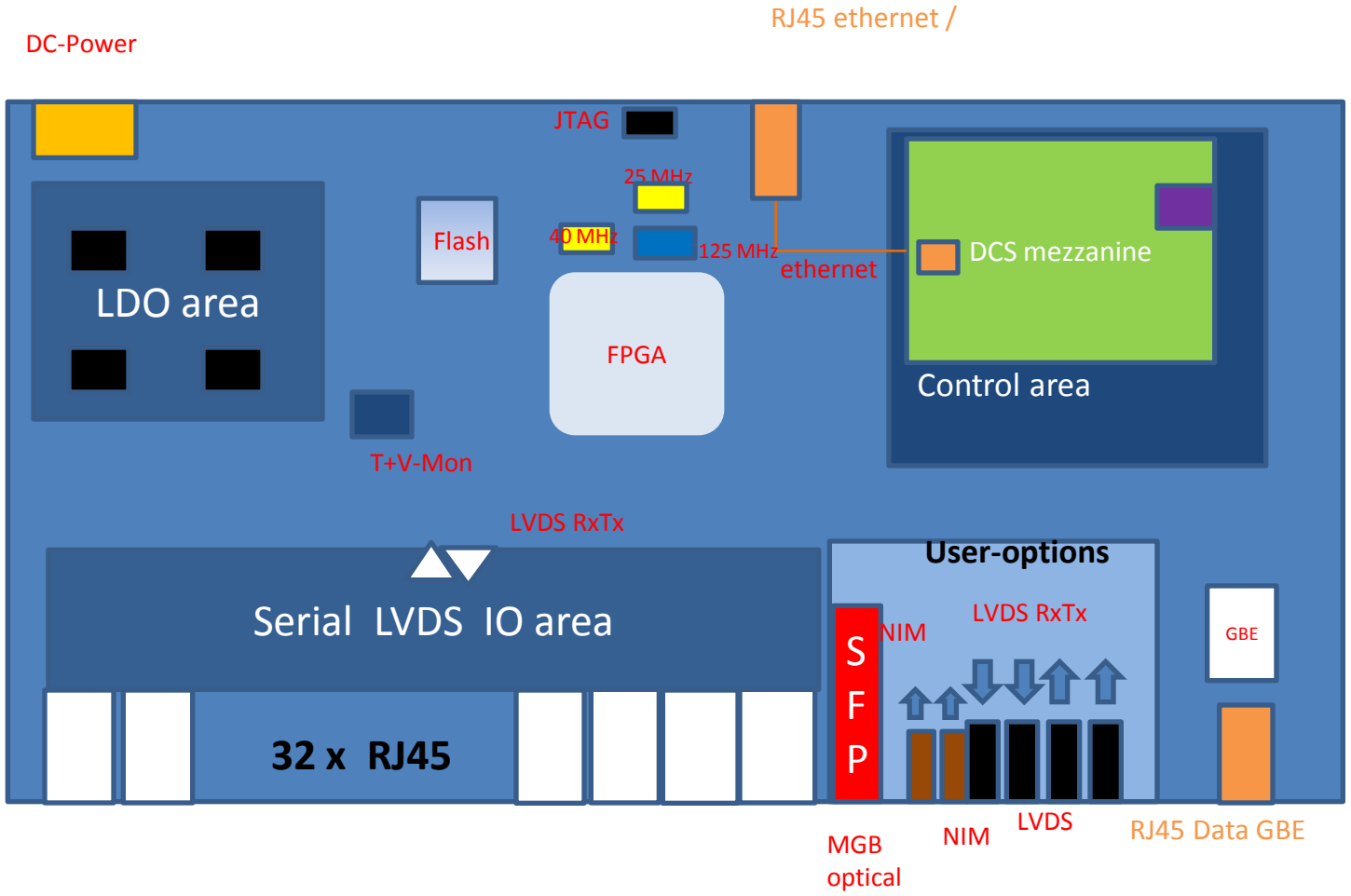


SRU architecture



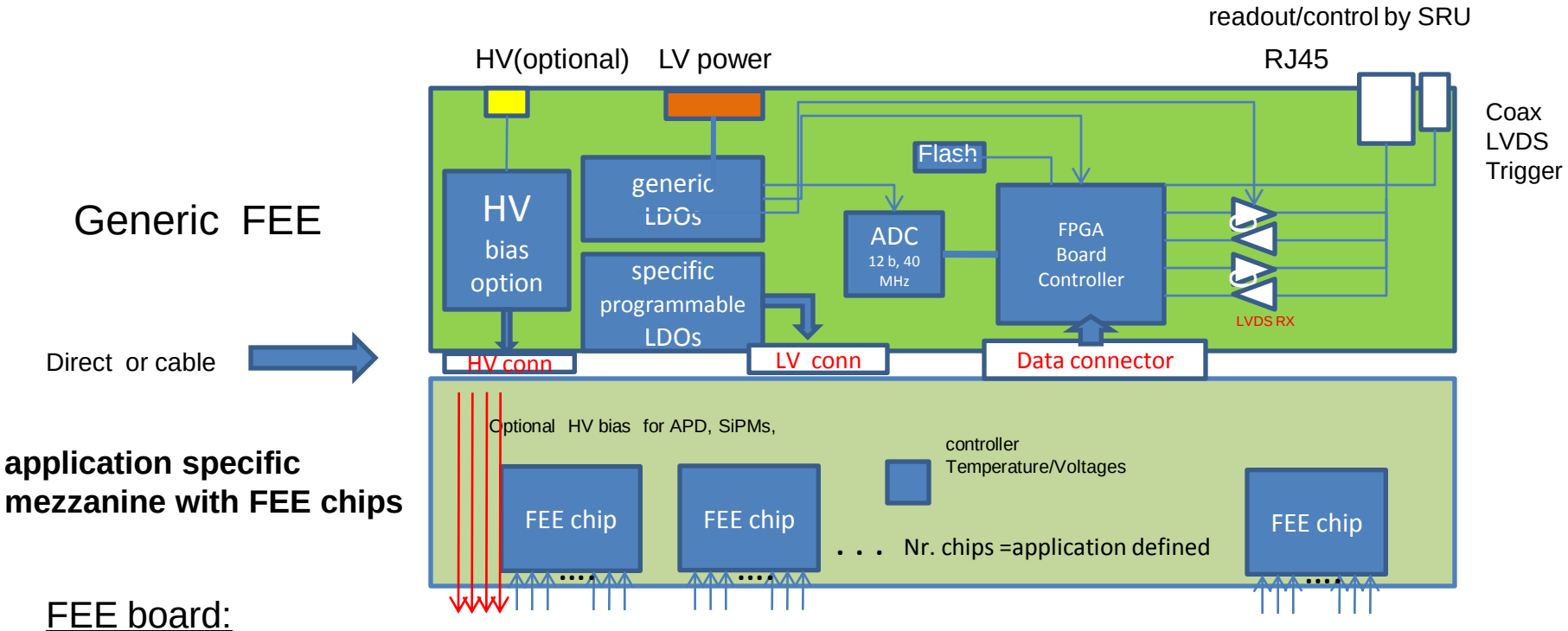
SRU card layout draft

based on similar LCU card of ALICE EMCal (started)



FEE card architecture

based on FEE electronics PHOS and EMCal



FEE board:

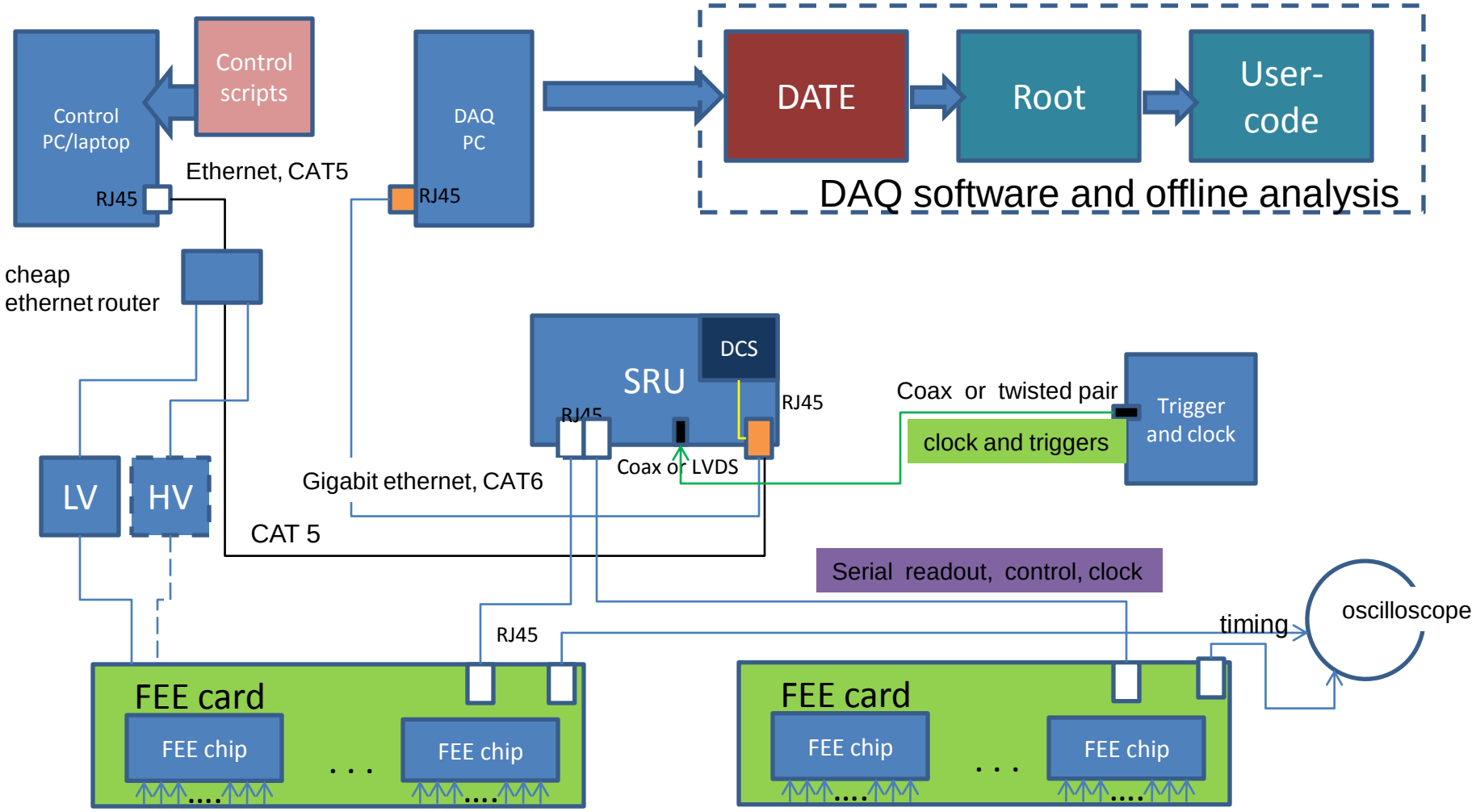
ADC= ADS5273 octal 70MHz , 12 bit ADC TI
FPGA = ALTERA ACEX EP1K100 or upgrade
FLASH = ALTERA EPC16QC or upgrade
LDO's = MIC29301 (3.3 V + 2.5 V, programmable)
HV bias = 12 bit programmable HV up 400V (option)
LVDS Rx = SN65LVDS100
HV connector = tbd
LV connector= tbd
Data connector = tbd

Mezzanine board:

FEE chips may contain:
Pre-amplifier / shaper /threshold /ADC
Controller = AD7417 Temperature, Voltages
Protection diodes for Gas detectors
HV filter for diode based photo detectors

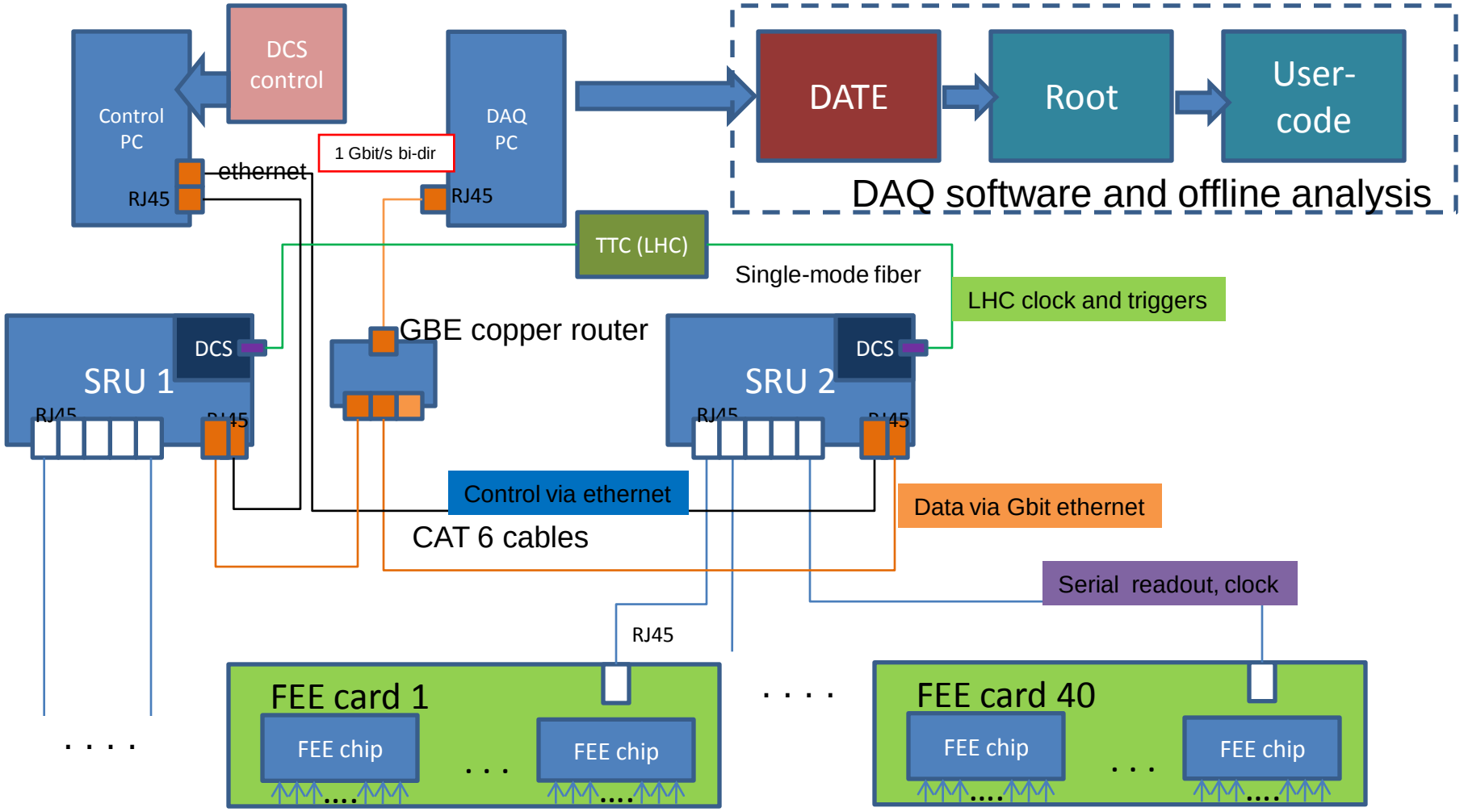
Test system architecture

1 SRU, GBE copper, User trigger+clock, control via ethernet/DCS



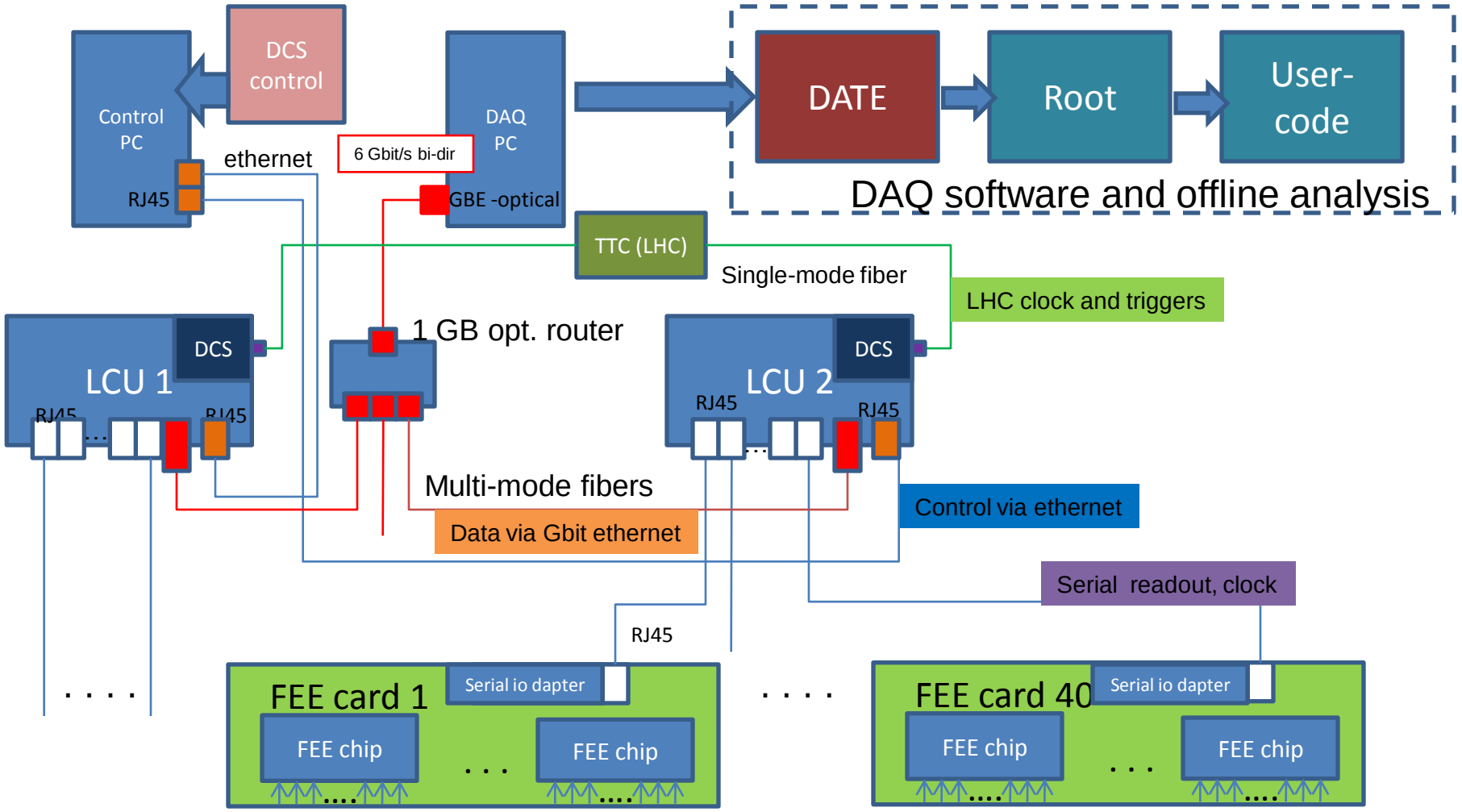
LHC low BW architecture 1

N x LCUs, GBE copper and router, TTC, Control via ethernet/DCS



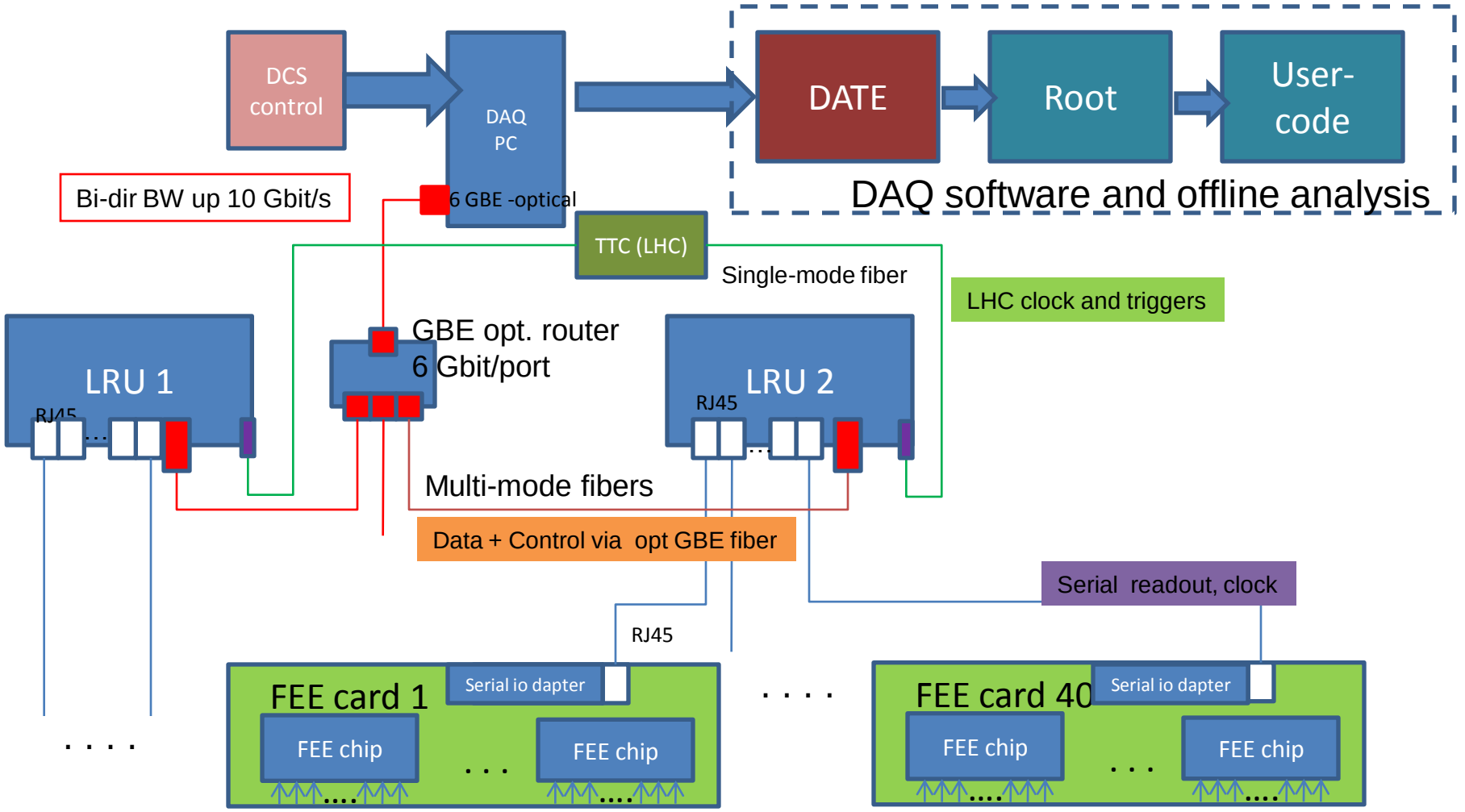
LHC high BW architecture 2

N x LCUs, optical GBE router, TTC, Control via ethernet/DCS

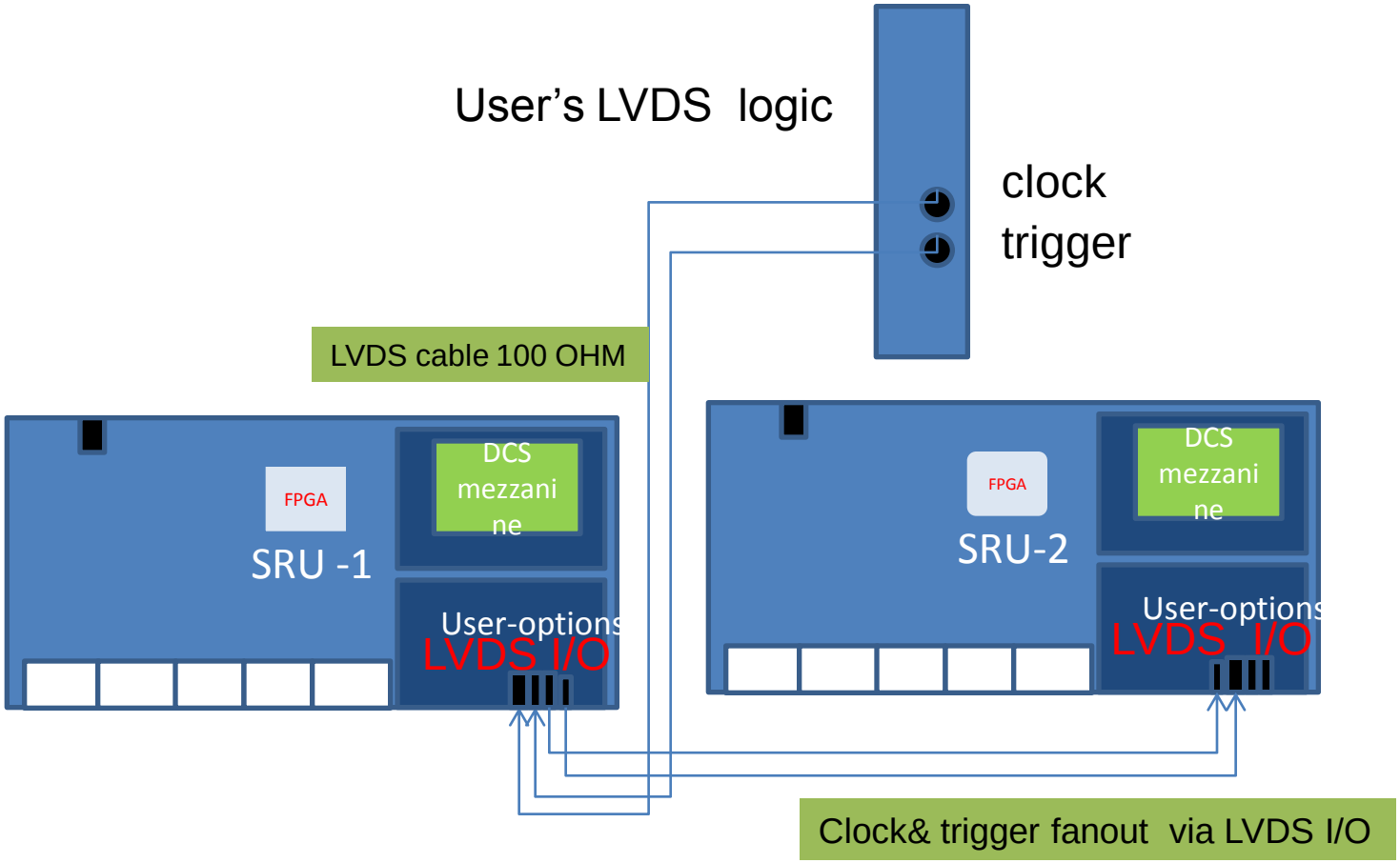


LHC high BW architecture 3

N x LCUs, optical 6 GB router, TTC, Control via GBE fiber

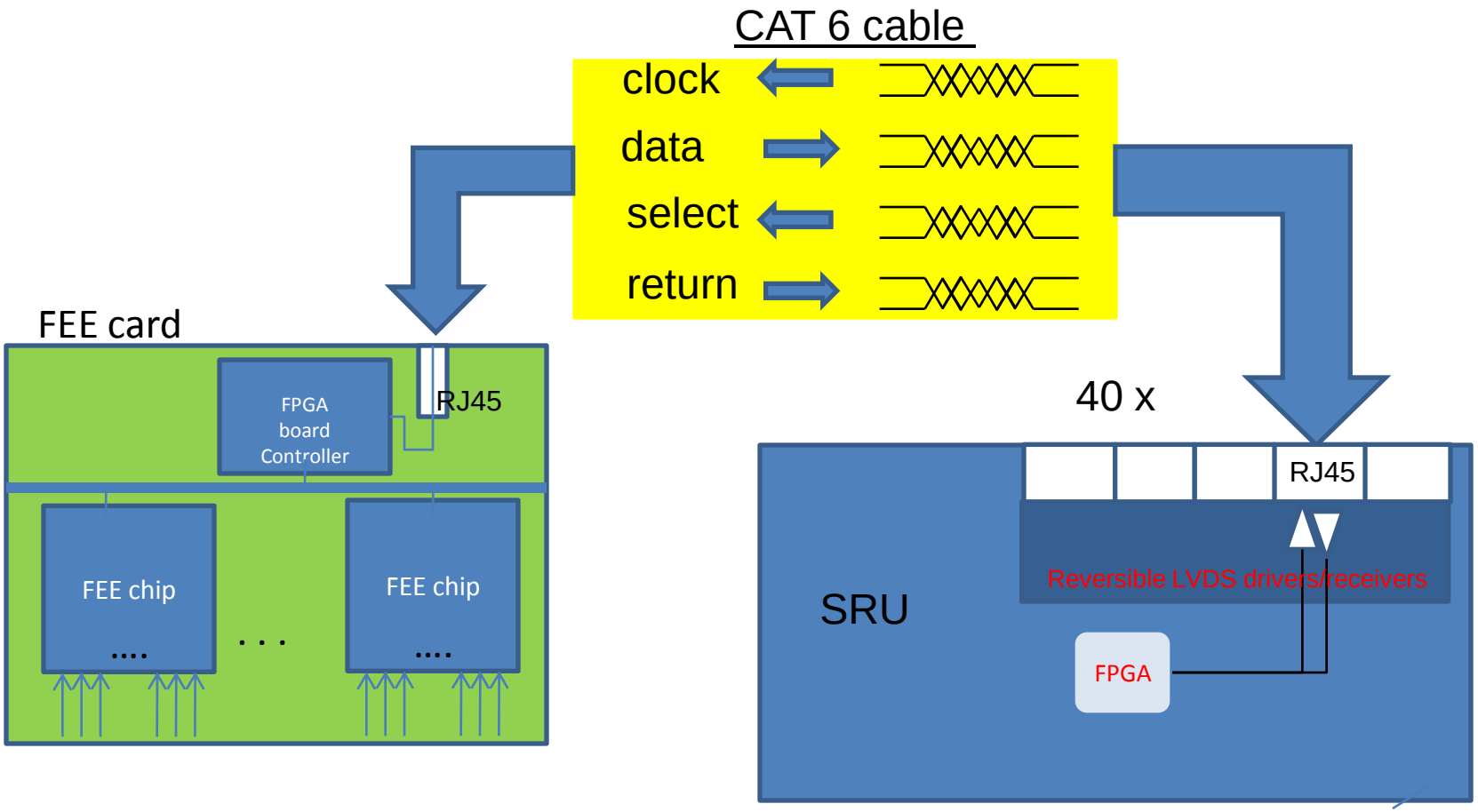


LVDS clock & trigger chain test systems without TTC



SRU<->FEE: serial LVDS

physical layer



Serial readout/contol modes

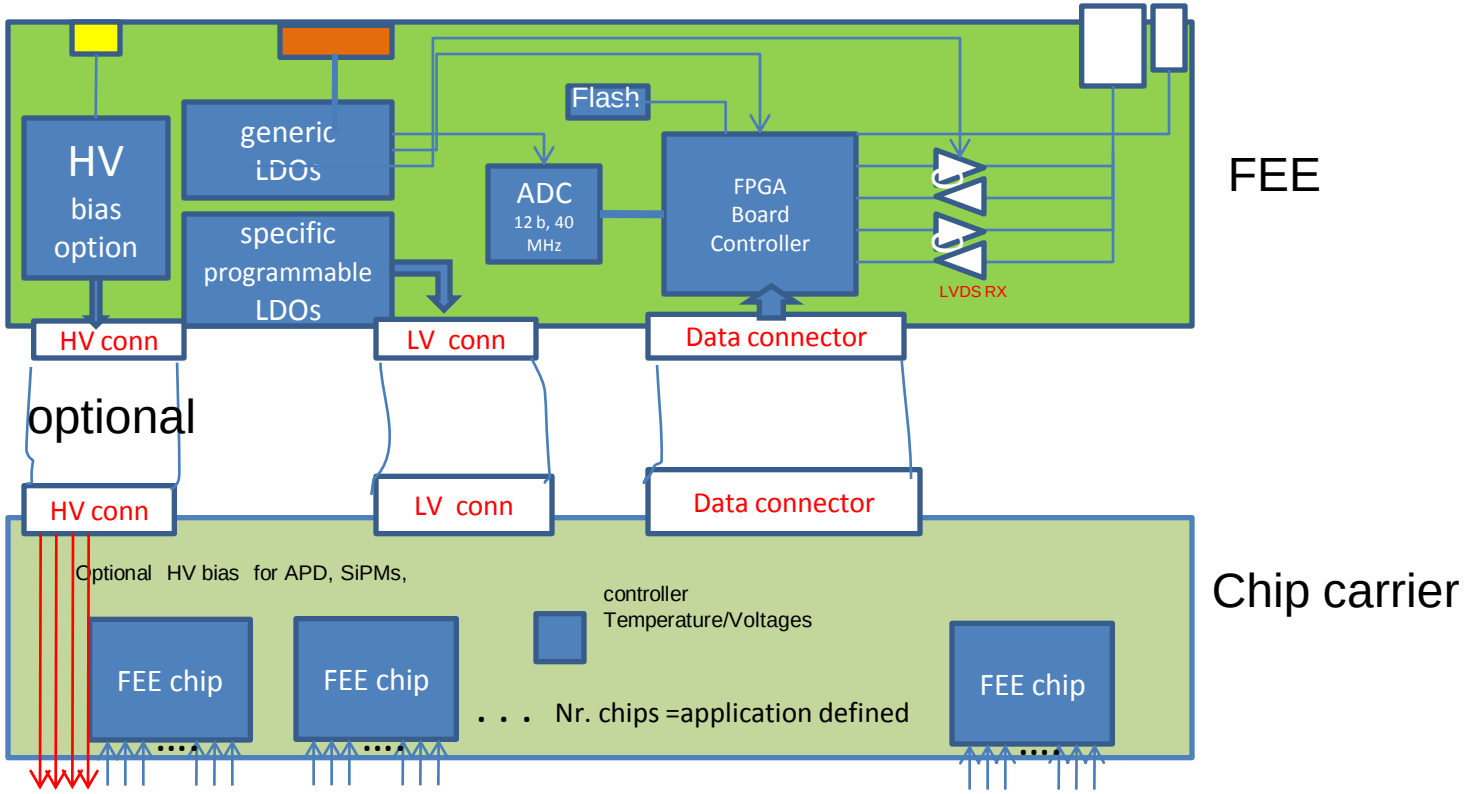
2 modes of operation defined by SCU clock
Board controller senses clock to switch mode

Readout mode: clock = 40 MHz (or other)
data = 200 Mbit/s
select = readout-trigger to FEE
return = local trigger from FEE

Control mode: clock <= 4 MHz
data = Serial data out
select = Serial data in
return = coded status

Chip interface

Standardize 3 type connectors: Low Voltage, Data & Controls, HV (optional)
Allow use of flexible cables or captons to connect chip carrier FEE



Frontend chips

Carioca (LHCb):
http://www.ca.infn.it/~gruppo1/notes/lhcb-2003-009.pdf
http://riegler.home.cern.ch/riegler/carioca.htm
current mode amplifier
12mV/fC at 50 pF, pos and negative
Min. charge 2fC at 50 pF (12400 e)
input impedance 50 Ohm.
1 bit ADC (= threshold), noise 2000 e + 50e/pF
8 channel chip, 360 mW

Beetle (LHCb)
http://indico.cern.ch/conferenceDisplay.py?confId=a022237
Charge sensititve preamp/shaper 23 ns peaking @ 30 pF
Analogue pipleline 160 samples to analogue readout amplifier (ext. ADC)
128 Individual 1 bit ADC comparators
Noise 500e +50e/pF
Dynamic range 110.000 e (2%)
128 channel chip (700 mW)
10 MRad hardness

SVX3D (CDF)
T.Zimmerman NIMA 409 (1998) 369-374

programmable gain
8 bit ADC, max 50 MHz
analogue pipeline
ADC ramp and comparator
frontend sensitivity 15mV/fC at 30 pF
noise 500e + 60e/pF ,
0.4 Watt per 128 channel chip
4 MRad hardness

" noname" (NIKHEF) 2008 test samples
http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=01009677
Made for GEMS + Micromegas gemacht (JFETpreamp inputs).
1 bit ADC (comparator), 100 MHz hit scalers.
noise 800 e +60e/pF
4 ns risetime at 10 pF input capacity
Signal/noise for 4 fC (25 ke) 10:1 for 35 pF (2500 e noise)
0.76 Watt per 32 channel chip. Fast Or.

Fontend chips continued

VFAT (Totem)
http://jinst.sissa.it/LHC/TOTEM/ch07.pdf
128 channels, Fast OR, 22 ns shaper + 1 bit ADC (comparator)->buffer
Trigger latencies up 6.4 us.
noise 650+50e/pF
Parameters via I2C

APV25 (CMS)
http://www.hep.ph.ic.ac.uk/cms/tracker/apv25_chip.html
LEB99 workshop proceedings, p. 162
" The APV deep submicron chip for the CMS Detectors Made for silicon strips"
128 channels, preamplifier 4.5 mV/fC
50 ns shaper,
192 deep pipeline sample memory @ 40 MHz
APSP deconvolution filter to extract amplitude and time
Serial differential output

SPIROC (ILC)
http://indico.cern.ch/getFile.py/access?contribId=53&sessionId=11&resId=0&materialId=paper&confId=21985
new chip for Si-PM's under test since 2007, 10k Channel demonstrator in 2009

2 charge preamps (high and low gain) programmable gain
2 programmable slow shaper 50 -175 ns for CSA memory
1 fast shaper 15 ns for discriminator

36 channel, 12 bit ADC for charge and time measurement
Different readout modes
16 deep analogue sample memory
Only 15 microwatt/channel ! in power-pulsed mode

PASA + ALTRO (ALICE)
Made for large TPC
http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc

PASA 16 channel shaping preamplifier
5mV/fC, dynamic range of 2V
rise time 120ns
shaping time (FWHM) 240ns
tail cancellation at the ~1‰ level after 700ns.

ALTRO only:
16 x ADC with baseline restore and ZS features
10 bit max 20 MHz
16 bit sampling pipeline, 512 deep Multi-Event Buffer
40 bit bus readout @ 40 MHz
0.25 W /chip

AFTER chip (T2K)
Made for TPC
http://indico.cern.ch/contributionDisplay.py?contribId=52&confId=16213
72 channels with CSA 120-600 fC adjustable
negative or pos input signal choice
Shaper 100ns – 2us adjustable
511 cells analogue storage
Slow controls interface,
Output buffer to external ADC
Readout 20 MHz

Implementation details

SRU: Xilinx Virtex-5: FXT

65nm family fabricated in 1.0v, triple-oxide process technology

480 User I/Os
4 -8 integrated MAC controllers
1- 4 PCI-e endpoint
8 -24 Rocket-IO GTX transceivers 6.5 Gbps
work with integrated PCI Express® endpoint and Ethernet MAC blocks
2- 6 DCM clock managers 550 MHz
2 PowerPC blocks

FX device with 665 pin BGA ~ 500 USD single unit, Avnet price Jan 2009
volume cost can be negotiated with Xilinx
like for previous projects, target 300 FS

Also existing: XAUI attachment unit for combining several GTX lines into 10 Gbps

Implementing data over GBE

The first MEP packet driver in FPGA for LHCb was written and tested by A.Guirao in 2003/4. It transferred error-free Multi-event data embedded in ethernet between an ORCA FPFA and a DAQ PC via an optical switch.

Phase A: For SRU data to DAQ via GBE copper (1 Gbit/s max)

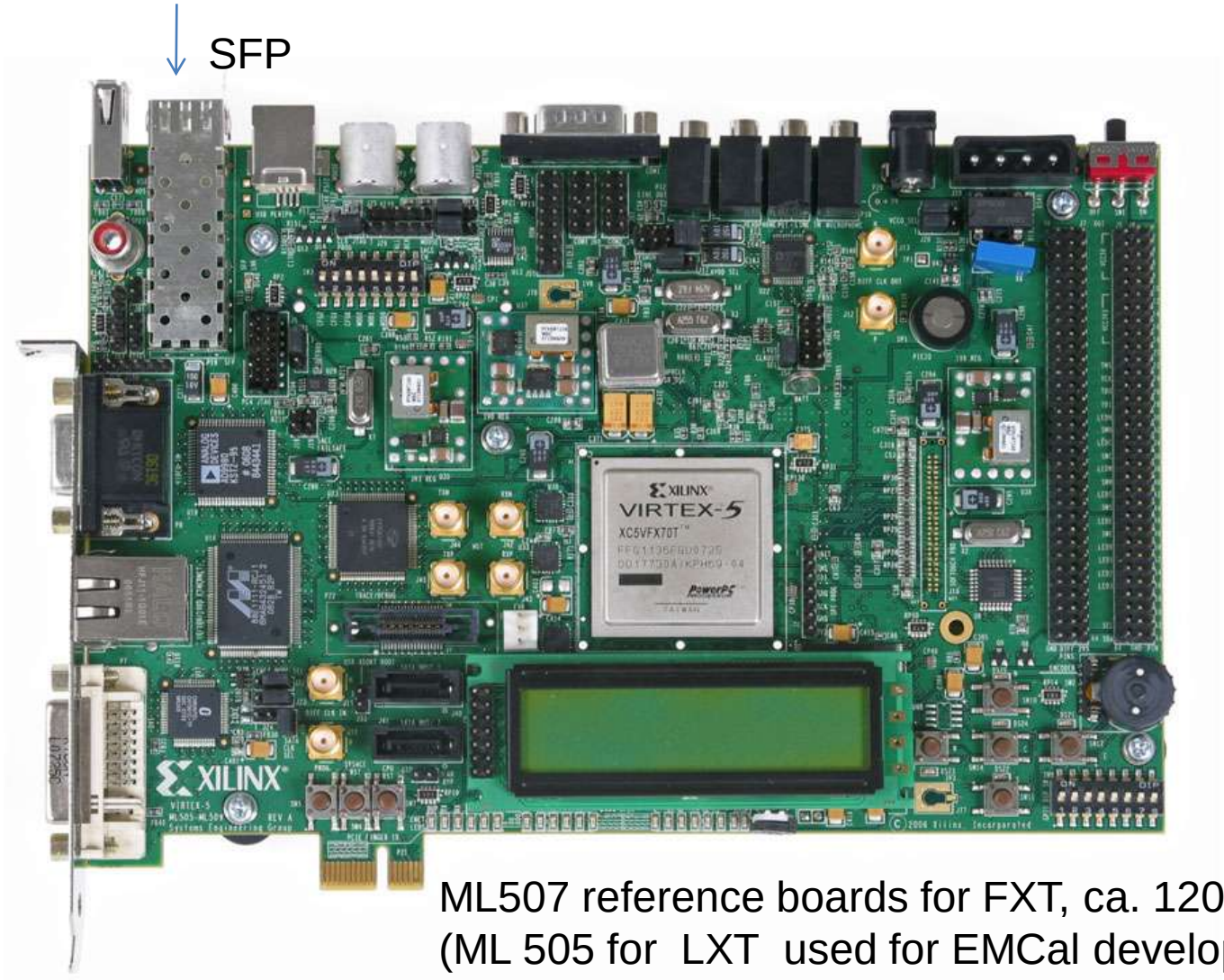
-develop an ethernet packet driver Virtex FPGA- > PHY chip (based on LHCb ?)
-embed in the IP payload the ALICE data format (Alice Int-2002-010 V11 , March 6 2007)
-Achieve stable transfers with BER measurements over 100 m CAT 6 cable

Most of this can be done with the Xilinx **ML505/6/7** development board before we have a first proto board (Target date for LCU march 2009)

Phase B: For SRU data to DAQ via 10 Gbit fiber (10 Gbit/s max)

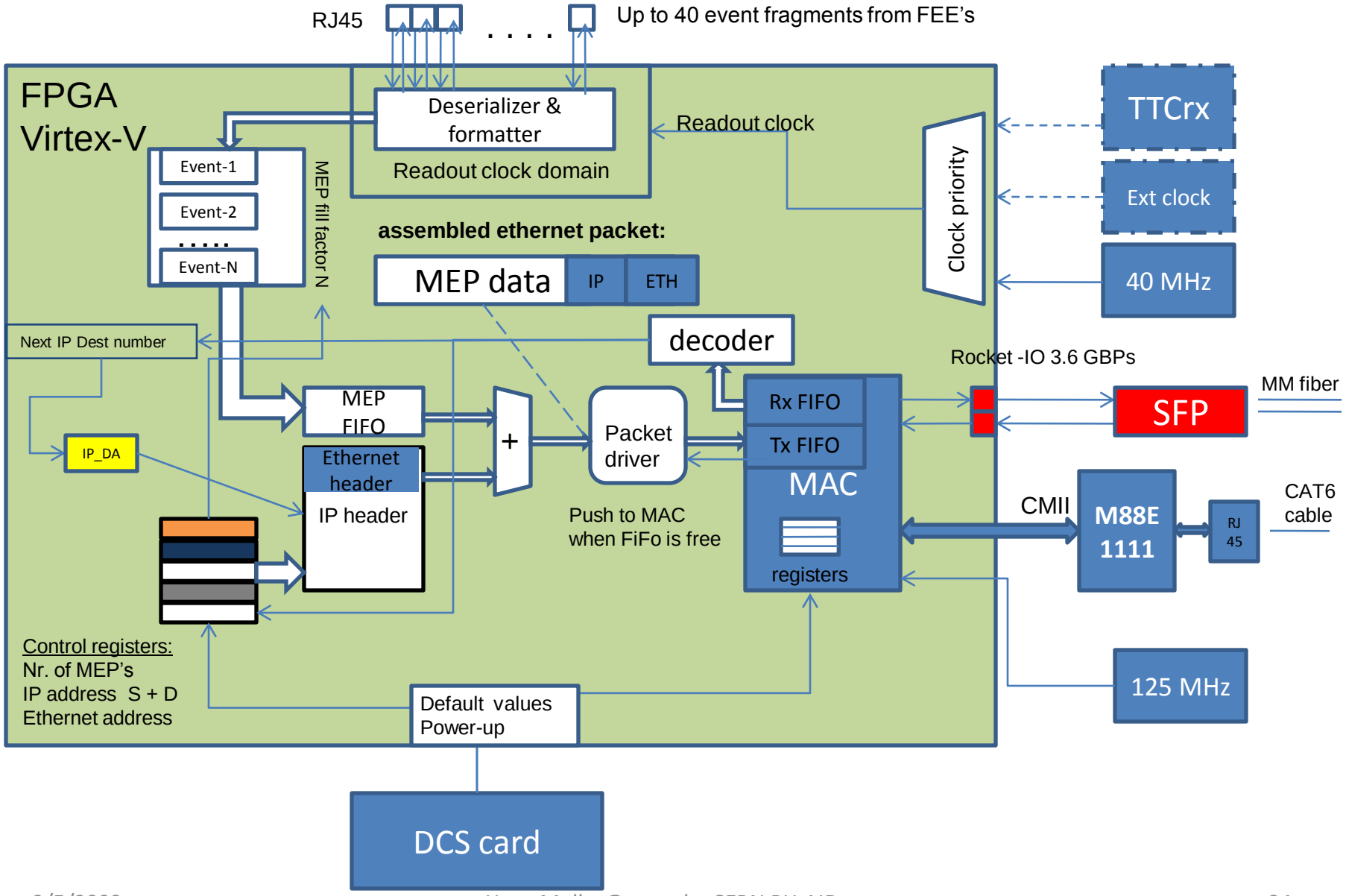
- use new LX50FXT with 6.5 Gbps GTX transceivers, probably 2nd version SRU
- acquire optical switch OC768 (48 Gbps)

development platform for FXT FPGA



ML507 reference boards for FXT, ca. 1200 USD
(ML 505 for LXT used for EMCal development)

IP packet generation in FPGA



IP header

Gigabit ethernet physical (RJ45) for phase A

Marvell Alaska single port Gigabit transceiver M88E1111

on LCU

Inside LX50T

Magnetics: inside RJ45 connector:
HALO HFJ11-1G01F

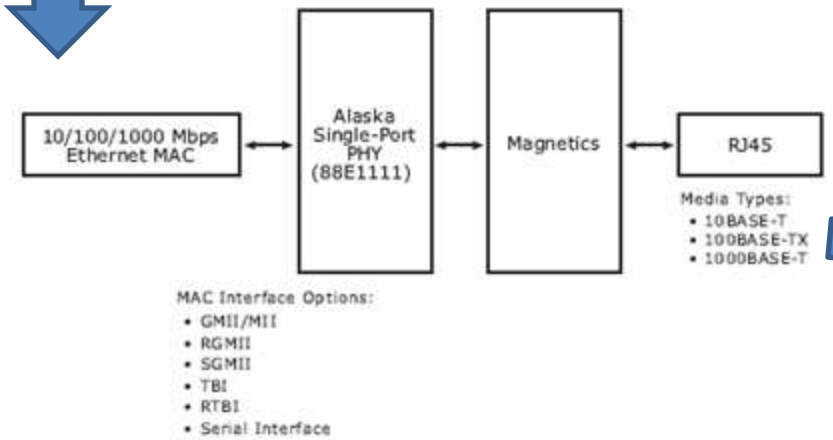
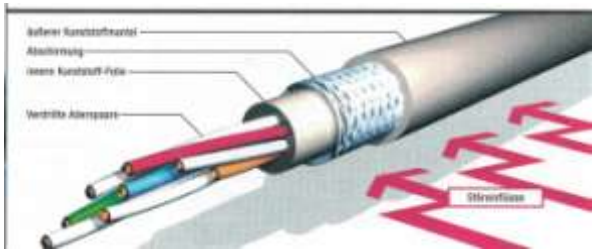


Fig 2. Alaska Single-Port GbE Transceiver (88E1111) Copper Applications Diagram

RJ45 on front

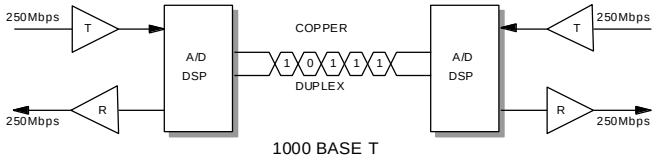
GiGabit Ethernet (GB) over copper

- Bididirectional over 4 twisted pairs 100 OHM
- 250 Mbit/s / pair in each direction clocked @ 125 MHz
- 5 level analogue PAM coding: 4* 125 MHz + 1 Error code
- Duplex GB operation = 2 * 1 Gbit/s
- 115 Mbyte/s max. BW per direction, reality up 85 Mbyte/s
- S/UTP cable = 1 single shield
- S/STP cable = 1 shield + 4 individual shields
- Cat 6 cable up 450 MHz
- Cat 7 cable up 600 MHz
- IEEE 802.3ab = GB over copper up 100m (BER ~ 10E-10)
- 1000BASE-T (copper) twisted pair CAT5e (or higher)



S/UTP cable

4 X



1000 BASE T

Eye patters Fast Ethernet 100BASE-TX and 1000BASE-T

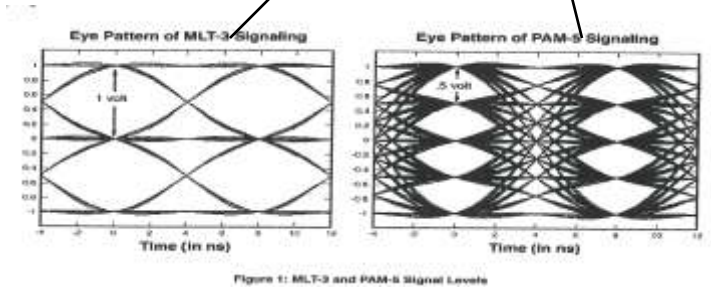


Figure 1: MLT-3 and PAM-5 Signal Levels

Gigabit ethernet over fiber

1000 BASE-SX (fiber) up 500 m over Multimode fiber (1 Gbit)
10 GBASE-SR (fiber) up 300 m over Multimode fiber (10 Gbit)

SFP + (Small Formfactor Pluggables)

Huihong Fiber:
SFP+ SR fiber transceiver module with 850nm VCSEL transmitter and PIN photo detector. IEEE 802.3ae 10Gbase-SR, electrical interface of the SFP+ SR is compliant to SFF-8431
max working distance is 300 meters over multimode optical fiber
MERGE Optics
SFP+SR TRX10GVP2010 GBE is a multi-purpose optical transceiver module for 10Gbit/s data transmission applications at **850nm**.

SFP+ RX/TX modules

20 pin SFP connectors

Multi-Mode fiber

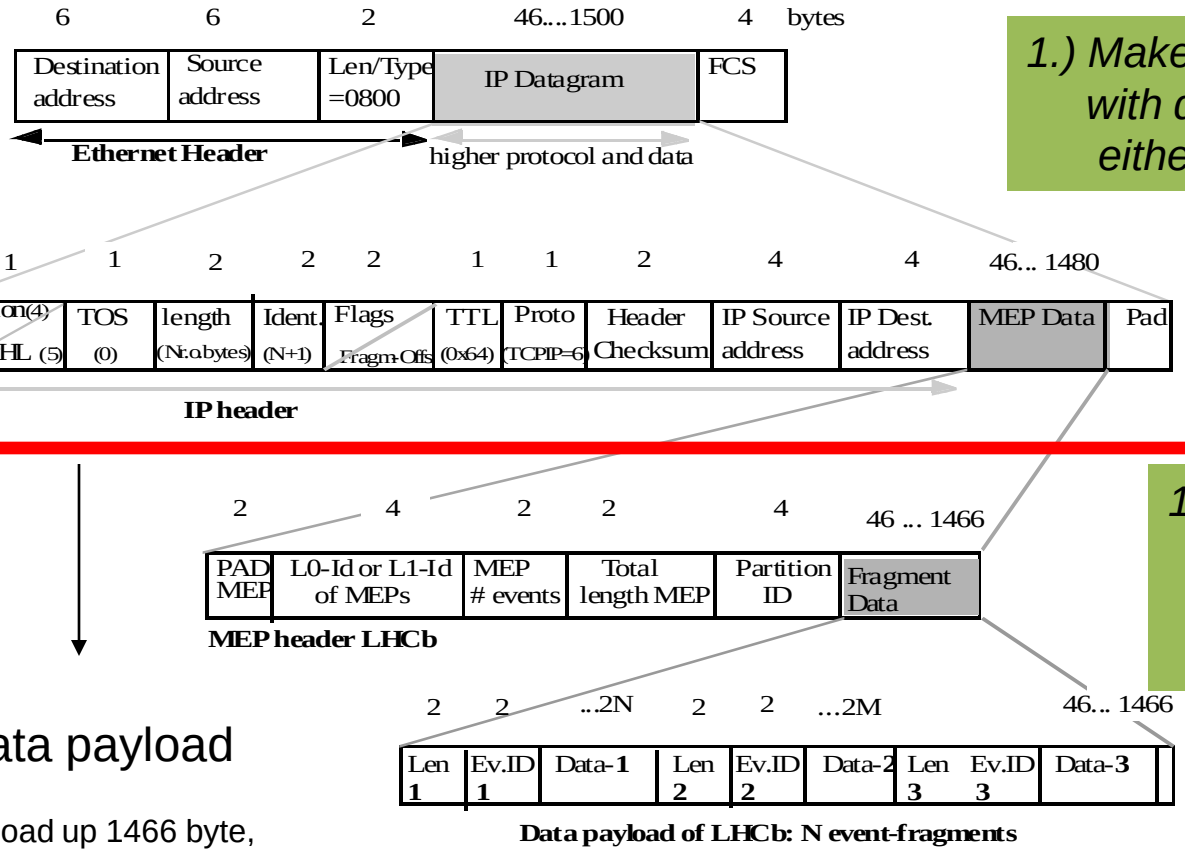
LC connector on LCU side
E200 connector on PC side

CERN SCEM 04.67.10.x00.0

Length max 50m

Multi-event data via Gigabit ethernet*

IPv4 Data Format (LHCb concept)



1.) Make IP packet frame in FPGA with destination IP address either fixed or received from DAQ

1.) Add data payload = event data user-specific format shown here LHCb format

Data payload

Payload up 1466 byte,
more with Jumbo packet supporting equipment , but may restrict choice of equiment

* LHCB note LHCb DAQ 2004-028

IPv4 packet generation in FPGA

Ethernet frame format for PMC3386 MAC

Bit position

31 28	27 24	23 16	15 12	11 8	7 0
MAC DA[47:40]		MAC DA[39:32]	MAC DA[31:24]		MAC DA[23:16]
MAC DA[15:8]		MAC DA[7:0]	MAC SA[47:40]		MAC SA[39:32]
MAC SA[31:24]		MAC SA[23:16]	MAC SA[15:8]		MAC SA[7:0]
L/TYPE[15:8]		L/TYPE[7:0]	Version	IP Header Length	Type of Service
Total Length[15:8]		Total length[7:0]	Identification[15:8]		Identification[7:0]
Flags	Frame offset[11:8]	Frame offset[7:0]	TTL		High-level protocol
header CRC[15:8]		header CRC[7:0]	IP-SA[31:24}		IP-SA[23:16]
IP-SA[15:8]		IP-SA[7:0]	IP-DA[31:24]		IP-DA[23:16]
IP-DA[15:8]		IP-DA[7:0]	Padding (0x00)		Padding (0x00)

Header

xample of frame

IAC DA 00 07 E9 17 83 00
IAC SA 00 00 00 00 00 00

00 07 E9 17
83 00 00 00
00 00 00 00
08 00 45 00
00 56 00 00
20 00 00 00
81 1C C8 00
00 01 C8 00
89 8A 00 00

IPv4

padding

00 00 00 00
00 00 00 01
00 00 00 02
00 00 00 03
00 00 00 04
00 00 00 05
00 00 00 06
00 00 00 07
00 00 00 08
00 00 00 09
00 00 00 0A
00 00 00 0B
00 00 00 0C
00 00 00 0D
00 00 00 0E
00 00 00 0F

Data start here
(32 bit up-counter)

Destination address assignment in FPGA:

10 bit destination address of a DAQ node:

A.) Test systems: 1 fixed address (part of initialization)
B.) DAQ systems with load scheduling: received via GBE from DAQ supervisor node

47

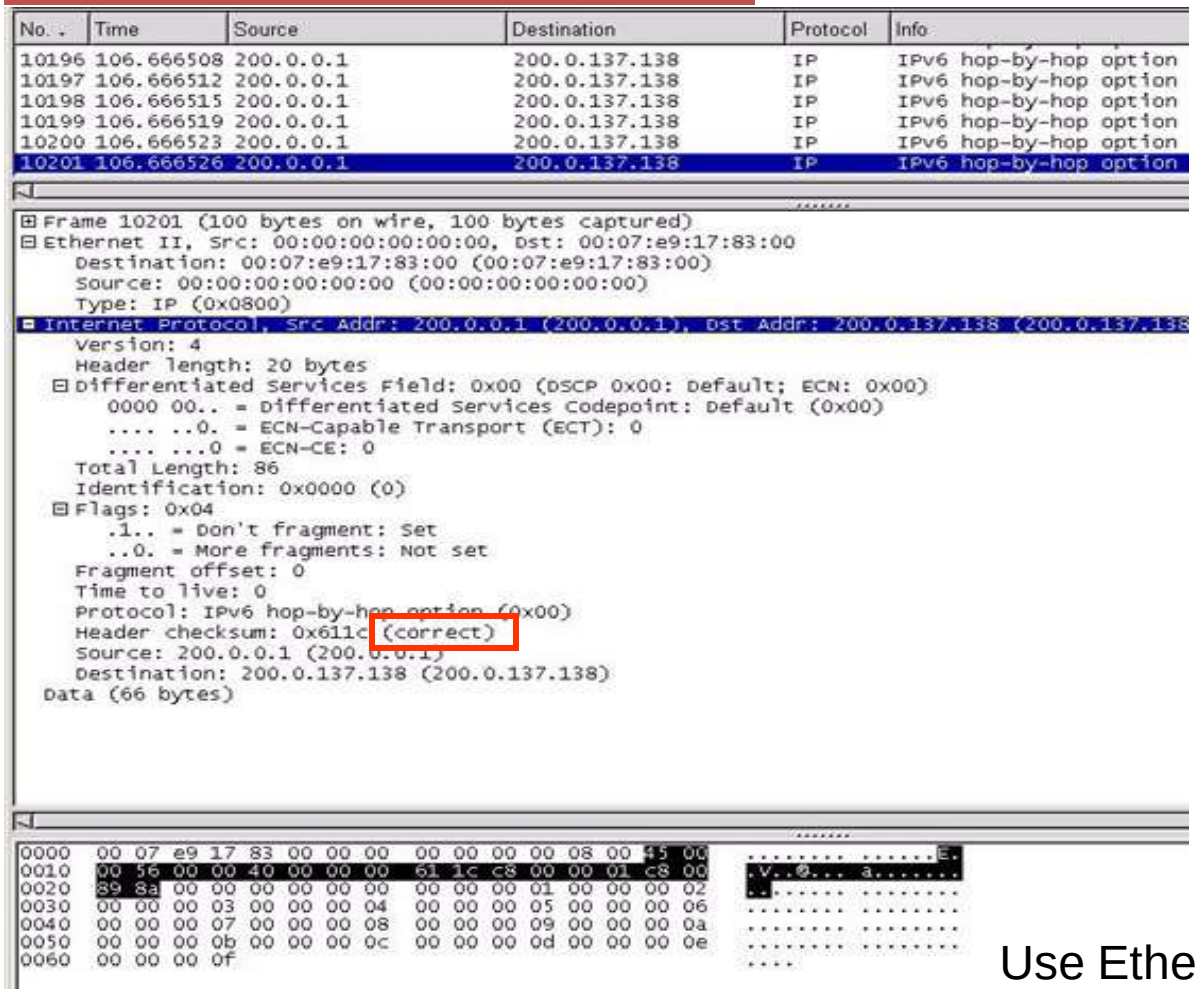
Ethern. dest. address	10 bit dest. address
IP dest address	10 bit dest. address

destinations:
max 1024 nodes
10 bit via GBE from
Readout Supervisor

First FPGA –made IPv4 packets

(LHCb, sept.'03)

Network sniffer on destination PC



FPGA encoding

Example of frame

MAC DA 00 07 E9 17 83 00
MAC SA 00 00 00 00 00 00

00 07 E9 17
83 00 00 00
00 00 00 00
08 00 45 00
00 56 00 00
20 00 00 00
81 1C C8 00
00 01 C8 00
89 8A 00 00
00 00 00 00
00 00 00 01
00 00 00 02
00 00 00 03
00 00 00 04
00 00 00 05
00 00 00 06
00 00 00 07
00 00 00 08
00 00 00 09
00 00 00 0A
00 00 00 0B
00 00 00 0C
00 00 00 0D
00 00 00 0E
00 00 00 0F

Use Ethereal to decode data payload

Board size: Rack mounting in 19”

PHOTO of TOR trigger board with
40 x RG45 and 4 LVDS
Plugs on the front panel

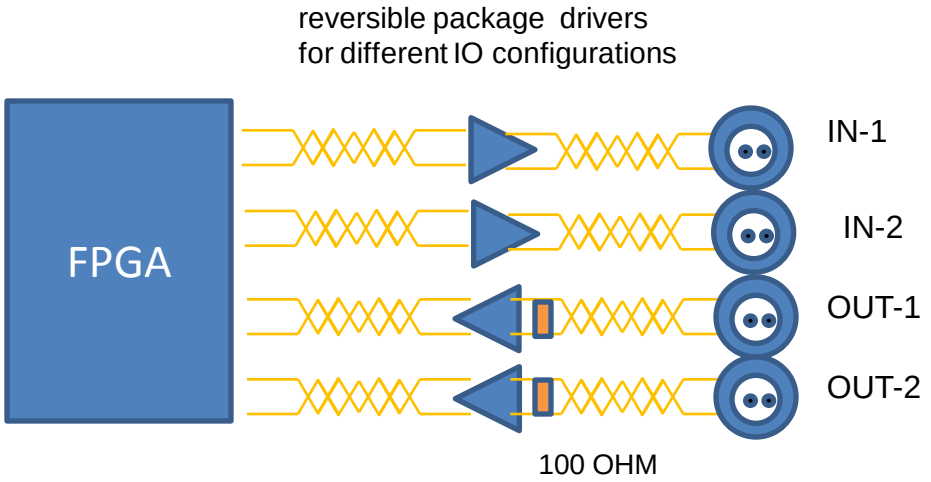
With similar layout, the SRU board will fit in 1U of a 19” chassis, power from backside

RG45 cables

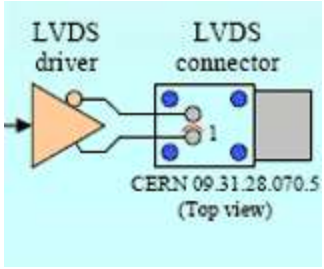
Trigger and clock cables

Bi-coaxial LVDS

Example:



Lemo size 00 B type
Cable plug
09.31.28.001.8



Tecnikabel (TO) –Italy -07w19 MCA 2 CERN IEC 60332-1
(1* twisted pair) 4.4 ns/m

SRU local clocks

Default system clock:

40 MHz Quartz oscillator 3.3 V , 40.0 MHz CFPS – 73 B (+-50 ppm) to be used as system clock only in absence of an external system clock (i.e LHC clock from TTC receiver). Auto-selection.

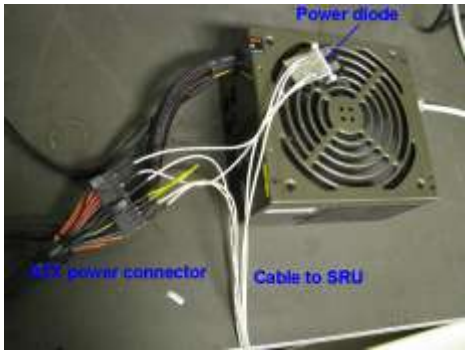
The system clock is transmitted to all RJ45 serial lines and can also be picked up from the RJ45 system clock output

Ethernet clock:

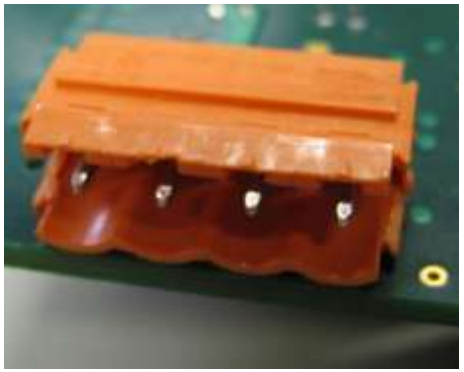
IDT Ethernet Clock Generator ICS844021I-01 which uses an 18pF parallel resonant crystal of 25 MHz for generating differential LVDS clock output with a RMS phase jitter @ 125MHz of 0.32ps (typical) @ 3.3V

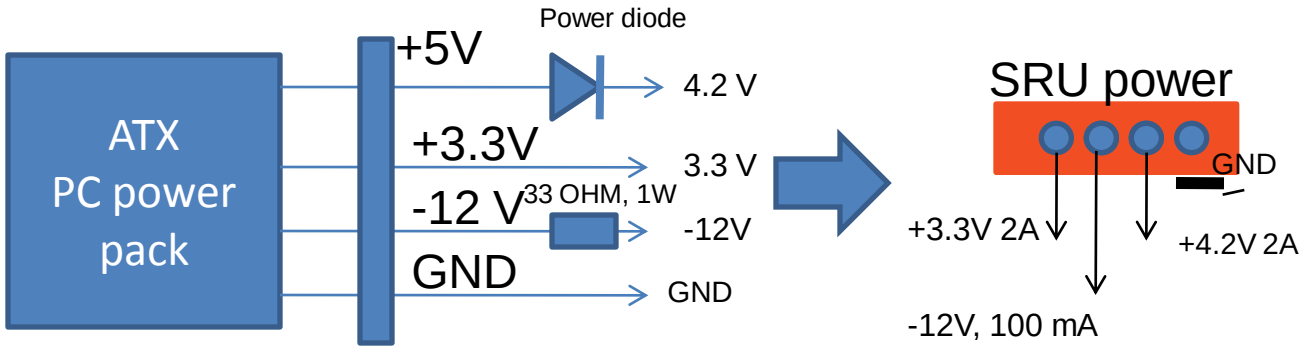
SRU power

The SRU supply voltages
can be derived from
a single ATX PC power pack



4 pin Weidmueller





ATX connector

Voltage regulators

Implement power sequencing, in particular switch DCS card 4.2 Voltca 1 s later than the Virtex.

Virtex-5 core: 1 Volt , 1.5 A

use TPS74401 from 2.5 V

Virtex I/O: 2.5 V, 1 A

use MIC29301 from 3.3V input

LVDS drivers, Flash, clocks, Physical chips, NIM-converter: 3.3V 1.5 A

use MIC29301 from 4.2 V

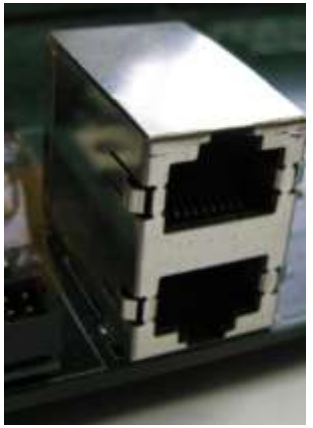
DCS mezzanine: 4.2 V direct from power connector

SRU-FEE connectors

<u>octal RJ45 blocks:</u>
on front for FEE serial readout

<u>dual RJ45 block (on back for options)</u>

Top: magnetic-free ethernet for DCS card
Bottom: LVDS system clock output (+ derivatives)

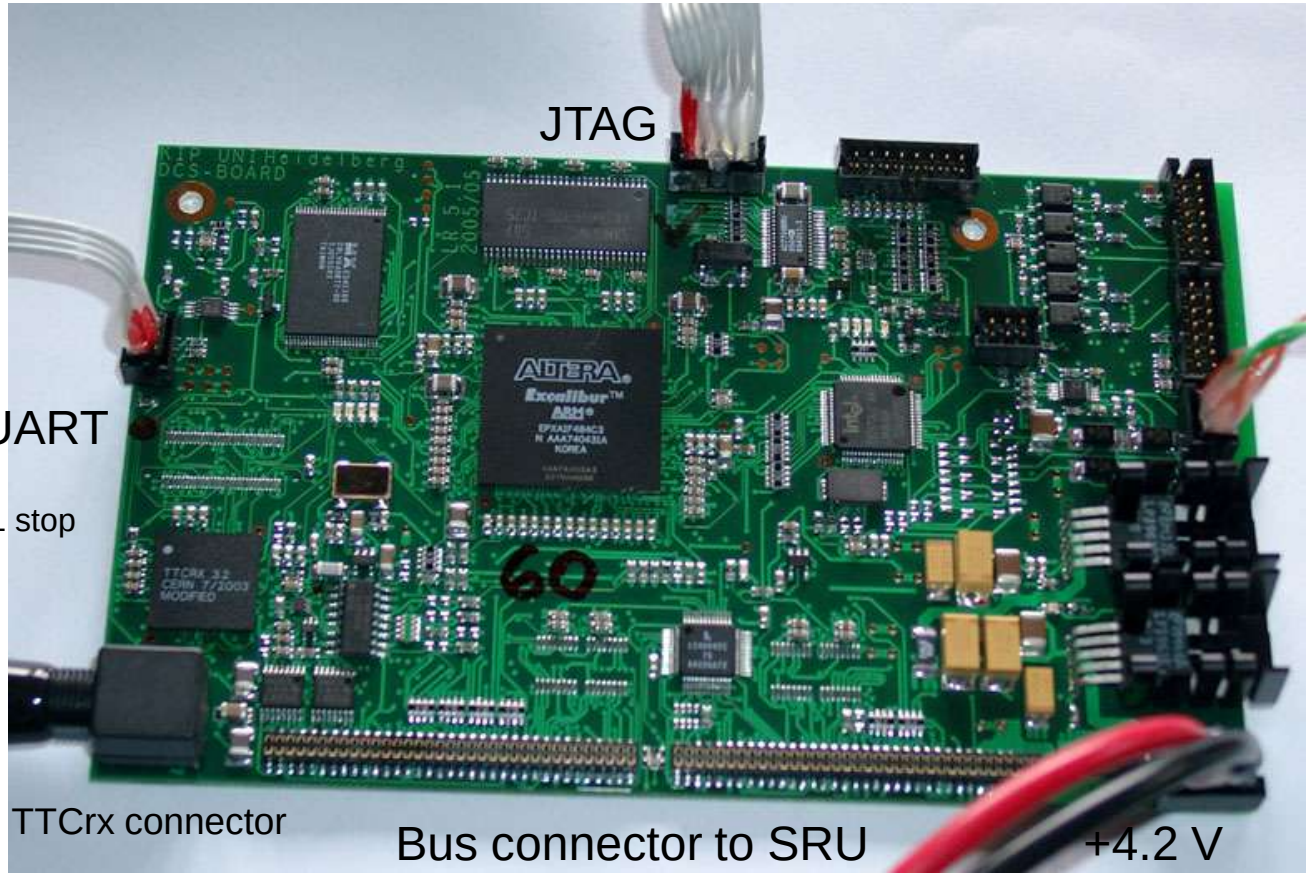


DCS card mezzanine option

KIP Heidelberg

http://www.kip.uni-heidelberg.de/ti/DCS-Board/current/

Standard DCS node for ALICE detectors: contains also TTCrx receiver



RS232 terminal
Baud 5700, 8 bit, 1 stop
no parity

Micro-Linux in Altera FPGA
Control shell for memory-mapped 32 bit bus
Remote login and NFS mount via ethernet

Problem: procurement of TTCrx (only for LHC applications)

FEE card

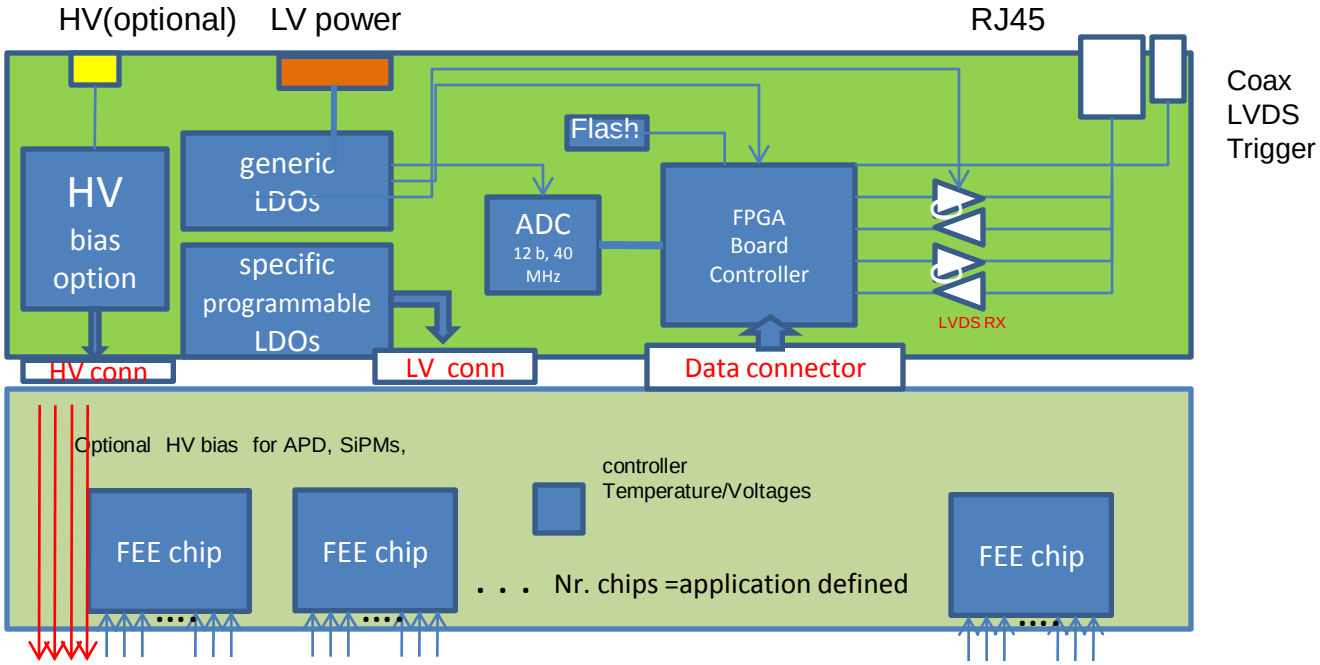
So far the FEE generic concept is drafted in a block diagram based on existing FEE cards, with local board controller firmware, current and temperature monitoring, digitization and buffering of data. Analogue and digital power, optional HV and control for solid state photo detectors

Generic FEE

Generic interface

Connectors:
Direct or cable

application specific mezzanine with FEE chips



FEE power

Low Voltages for FPGA and LVDS 3.3 and 2.5
Programmable Voltages for chip carriers
also negative

Note that LHC applications must be magnetic free
i.e. switching regulators don't work
Use low dropout regulators
Provision for cooling the FEE board
Temperature and current monitoring via Board controller

High Voltages: (up 400 V, 5 mA for APD users)
10 bit programmable range per channel for
APD and Si-PMs, also bias Voltages for Photo Diodes

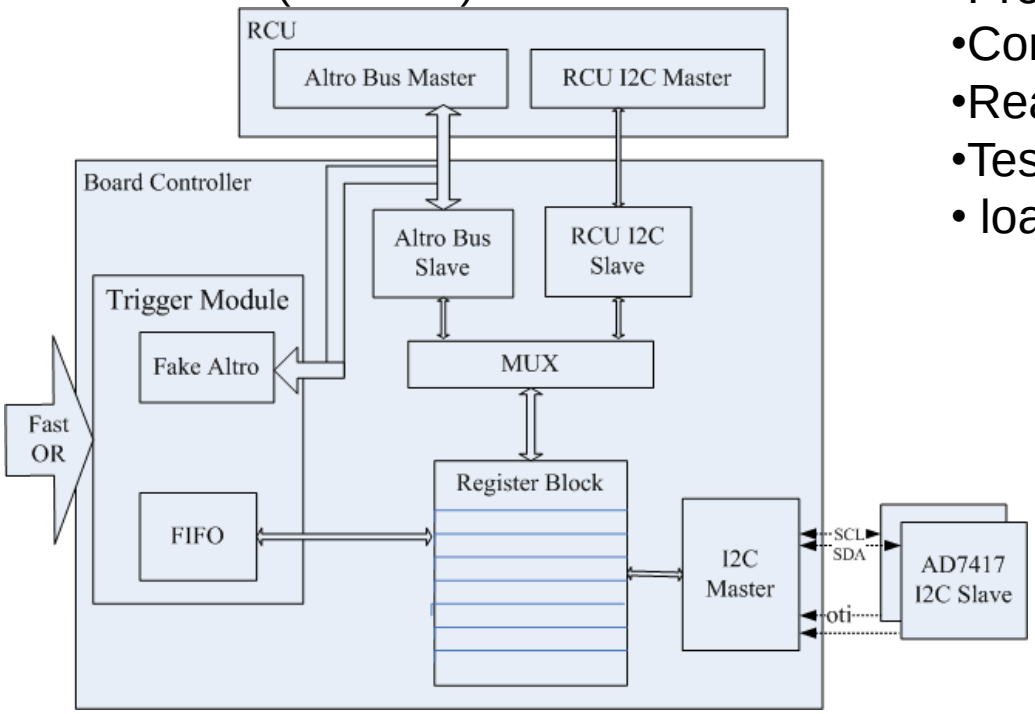
FEE<->CHIP connector

There are good and bad connectors, don't choose by catalogue, choose from lessons learnt.

- LVDS for digital signals: how many max?
- Chip Power and grounds: how many max?
- HV option: how many max?
- Analogue signals : how many max ?
- Other signalling standards, which ?

FEE Board controller

Block diagram of BC firmware in the EMCal TRU card (Virtex -5)



BC firmware, FPGA resident

- Configure operation of the FEE card
- Programmable HV and LV settings
- Configuration for frontend chips
- Readout of temperatures
- Test modes
- load data

CHIP carriers

Each chip carrier will be specific for application and for the choice of a chip

The interface to the FEE requires a standard connector pinout and a signalling level that is implementable with cables and /or connectors

-Grounding requires special care to prevent from noise
  separate analogue and digital grounds
  provide a single ground point
  differential input trace routing up to detector
  protection diodes for gas detectors

-Power and HV filtering
 local charge capacitors to sustain preamp loads

Case study: Carrier for Altro chip

I will do this based on our PHOS / EMCal FEE cards with Altro chips , Hans M.

CASE study: AFTER chip

This chip comes already with a complete readout system via Gigabit Ethernet and FEE cards, and therefore represents an excellent template.

Plans for use in AtlasMMega project as upgrade for the current Altro solution

Expect manpower from Atlas MM for case study

Short term Plans

For SRU development, use EMCal LCU and TRU design and Xilinx ML505 development system as prototype for SRU development

Status Jan 2009

-implementation of DCS card protocol on Xilinx LXT50 platform for control over CAT6 cables (done)
- transmission of data at 200 Mbps over CAT6 cables LVDS (done)
- decoding of TTCrx signals and transmission via 24 RJ45 lines to remote boards (ongoing)
- LCU board Cadence design (started)
- test of IP packet reception for DATE system (started)
- generation of IP packets in Virtex 5 with Alice common data header (planned)
- case studies for common chip interface based on Altro and After chips (to be started asap)
-define interface and connectors for chip carriers (to be started asap)

Longer term plans (2009)

Design FEE board and board controller

Choose a chip and design a chip carrier for the FEE

Test the first SR proto system in laboratory, based on GBE and DATE

User Interface for Controls of test system

Set up in testbeam (candidate Mmega project)

Provide a set of Root Analysis package for standard mesurements