Discussion on portable multichannel systems for MPGDs

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Outline

Introducing my research group

RD-51

- WG 5.4 The goal
- Design requirements for a portable multichannel DAQ system

My intention is to present my group, share a few ideas and start a discussion on the DAQ





35,000 students
2,500 researchers
Science park
Campus in 3 cities

Digital Systems Design Group

Five motivated engineers with CERN background...

- Angel Sebastiá (DELPHI DAQ)
- Francisco Mora (LHC DAQ)
- Raúl Esteve (ALICE ALTRO)
- José Toledo (LHCb DAQ)
- Jorge Martínez (PET tomography DAQ)



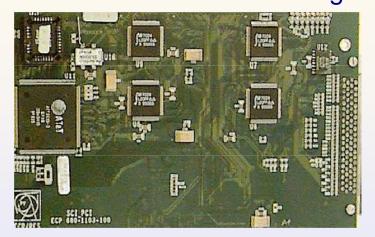
What are we good at?

DAQ systems for HEP, Nuclear physics and Nuclear medicine

Some examples of designs from our stage at CERN...(F. Mora PhD thesis)

Study of application of SCI to DAQ at LHC (CERN RD24)

VME-SCI and PCI-SCI bridges



WVME 1603 LynxOS 3m SCIRing 200 Mbyte/s

Sender Sender PMC2 MVEM1604 LynxOS 3m NVEM1604 LynxOS 3m Receiver PC 2m Intel PC Linux or W95

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 47, NO. 2, APRIL 2000

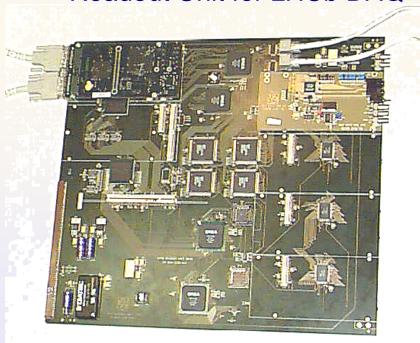


What are we good at?

DAQ systems for HEP, Nuclear physics and Nuclear medicine

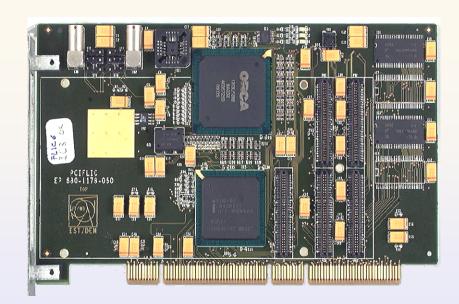
Some examples of designs from our stage at CERN...(J. Toledo PhD thesis)





IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 49, NO. 2, APRIL 2002

PCI DAQ card for NA-60 at CERN



IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 49, NO. 3, JUNE 2002



What are we good at?

DAQ systems for HEP, Nuclear physics and Nuclear medicine

A design for ALBA, Barcelona synchrotron...

HM5 – Histogramming module for MWPC



IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 51, NO. 4, AUGUST 2004 NUCLEAR INSTRUMENTS AND METHODS A 570 (2007) 511–517

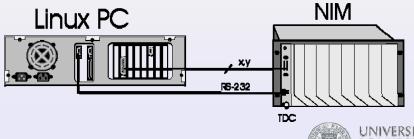
Used at:

BM16 at ESRF

Adam and Eva at Institute Laue-Langevin Max Planck Stuttgart

U. Copenhagen Denmark

ALBA Synchrotron Barcelona

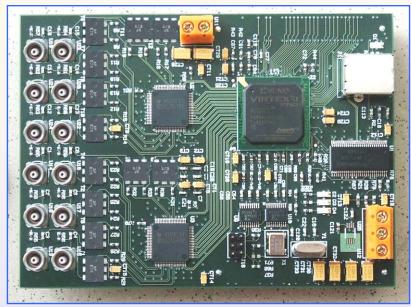


What are we good at?

DAQ systems for HEP, Nuclear physics and Nuclear medicine

A nuclear medicine project...(J. Martínez PhD thesis)

Planar Positron Emission Mammography (PEM) Scanners



NUCLEAR INSTRUMENTS AND METHODS A 537 (2005) 335–338 NUCLEAR INSTRUMENTS AND METHODS A 546 (2005) 28–32

Coincidence and Processing Module

- Free running sampling approach
- On-board processing and parameters extraction



What are we good at?

DAQ systems for HEP, Nuclear physics and Nuclear medicine

Two nuclear medicine designs...

Novel DAQ system for a PET tomograph

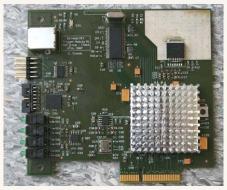


Half-size chassis



TRIG + DAQ in custom backplane







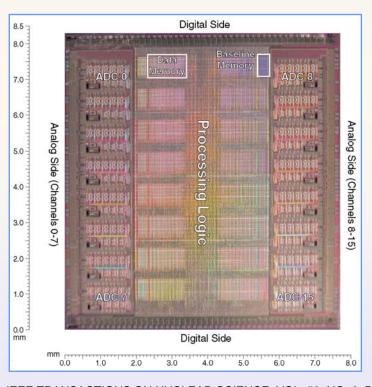
DAQ board

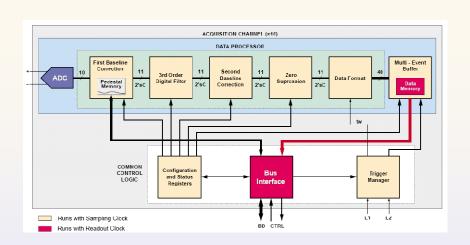


What are we good at?

ASIC design (R. Esteve PhD thesis)

Major contribution to the design of the ALTRO chip





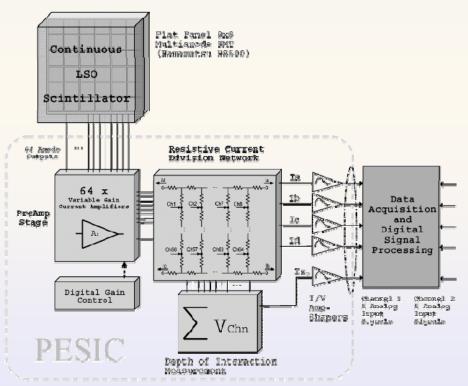
IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 50, NO. 6, DECEMBER 2003



What are we good at?

ASIC design

A second example... PESIC: An integrated FE for PET applications



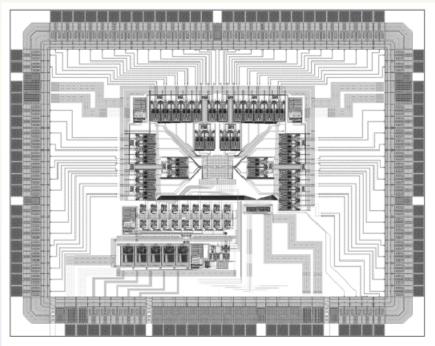


Fig. 2. PESIC (64 anodes version). 3.3 mm \times 2.8 mm in 0.35 μ m technology.

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 55, NO. 1, FEBRUARY 2008



RD-51



WG 5.4 - The goal

Scope (from RD51 Proposal)

"For the classical configuration of charge collecting pads or strips an easy-to-use portable readout solution will be developed"

Task and deliverables

- "Design and construction of portable multichannel systems"
- Deliverable: "Prototype system"
- Scheduled for m1/m12!!
 - WG 5.1 (Definition of FEE requirements) is m6/m12, m12/m36!!



WG 5.4 - The goal

...so, I understand the goal is to:

 Design a scalable, flexible and reconfigurable DAQ platform that can work with existing ASICs, trying not to reinvent the wheel

"All DAQ systems are by definition beyond the state of the art. No one designs a new one when an old system can can be adapted or upgraded to do the job"

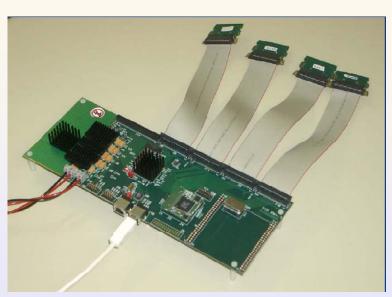
(...said once a senior scientist from Fermilab)

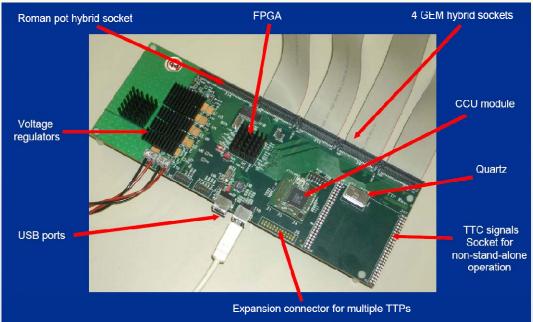
2. Wait for advances in WG 5.1 and, if required, adapt the DAQ platform to new requierements and/or ASIC



From April's meeting:

- TTP card: offered by Paul Aspell in April'08 in Amsterdam
 - Interface for 4 VFAT2 GEM hybrid boards
- We may to extend the TTP concept to a flexible, scalable DAQ that can be used for all ASICs







Binary readout

CARIOCA (8 ch) ASDQ (8 ch) VFAT2 (128 ch)

~ easy or direct interface to digital logic (LVDS)

Digital readout

ALTRO (16 ch)

~ direct interface to digital logic

Analogue readout

APV25 (128 ch)

Requieres external ADC

We could use existing FE cards and cabling for these ASICs and design a flexible DAQ to control them



3 ASDQ on a board



2 ASDQ + TDC on a board

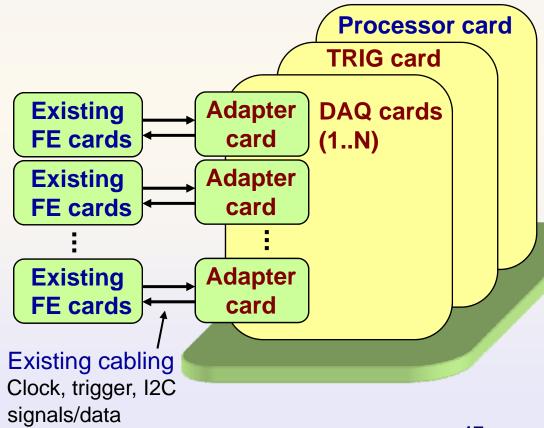


- N * ASICs on existing (?) FE cards close to the detector
- Existing power modules for FE cards
- Portable DAQ system
 - Scalable: modular system, single or multi chassis
 - Flexible: Input connectors, buffers, level conversion, etc. can be installed on application-specific mezzanines
 - Reconfigurable: FPGAs for FE control and readout, clock and trigger generation
- Common DAQ software



Adapter cards (application specific)

- Adapts connectors
- Digital readout (buffers, level conversion)
- Binary readout (buffers, level conversion)
- Analogue readout (+ ADC)



DAQ cards

- FE readout and control
- Data formatting
- FPGAs for flexibility
- p-p links to TRIG card
- Optional data input from other chassis

TRIG card

 Clock and trigger generation and distribution via p-p to DAQ cards and/from other chassis

COTS processor card

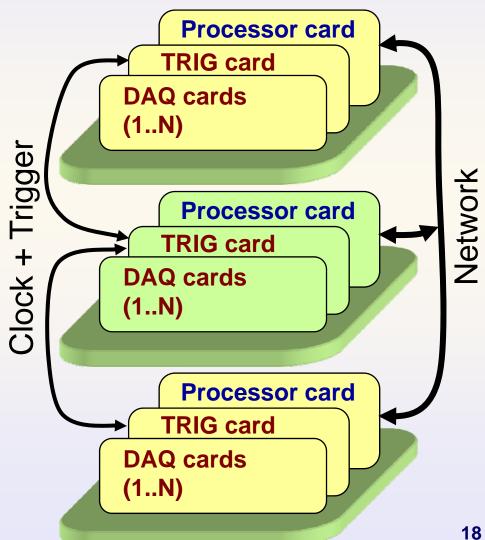
- Network interface
- Runs DAQ Software
- Reconfigures FPGAs

COTS chassis and backplane

- Power
- Backplane
- Mechanics



Only for large systems...



"Any path that narrows future possibilities may become a lethal trap" from the novel Children of Dune

Multi-chassis systems

- No special HW is needed
- One Master chassis
- CLK, TRIG distributed from TRIG Master to TRIG slaves
- DATA to Master via:
 - Network, or
 - one DAQ card per Slave send data to DAQ card in Master



- Re-use of existing FE cards and cabling
- There must be out there some existing DAQ HW we can adapt
- There must be out there some existing DAQ SW we can adapt

The concept is flexible, scalable and reconfigurable and aims at reusing existing developments

WG 5.4 scheduled for m1/m12

Discussion and feedback is needed

Thank you for your attention!

