Development of the CARIOCA Front-end Chip for the LHCb Muon System

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June 10 2003

*Para todos los que han hecho
de mí una persona mejor.
Con todo mi cariño.*

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Abstract

CARIOCA is an 8 channels ASIC developped as readout electronics for the
LHCb muon system detector. CARIOCA is a radiation hard ASDB chip (Amplifier Shaper Discriminator Baseline restorer) built using the IBM 0.25 μm
CMOS technology.

This Master's Thesis describes the work done on the last three prototypes
of CARIOCA. This is presented by showing the results related with the full
characterization of the 8th prototype of CARIOCA and how they relate with
past and future prototypes.

Acknowledgements

I have so many reasons to be grateful to so many people that I am afraid I will forget somebody on the way. I sincerely apologize for any possible oversight. I owe you a coffe it this is your case ;).

I wish to thank all the people at CERN with whom I have collaborated during the realization of this thesis. Not only for helping me in technical and scientific issues, but also for making me feel at home here.

Special thanks to my supervisor at CERN, Werner Riegler, always available to answer my thousands of questions. I have to find out who in Human Ressources assigned me such a nice boss and send him/her a box of chocolates. It has been a pleasure working and sharing office with him. Monday mornings have not been so hard this year :).

Nicolas Pelloux deserves also a big thank you. It is very gratifying working with somebody as generous in sharing his knowledge as him.

My warmest thanks to all the persons that have taken the time to teach me something.

As for the personal acknowledgements, I could fill up pages and pages with names of friends and relatives. Therefore, I will only mention "the highlights of the year". Ángel González, my grandfather, he always makes me feel very special :). Hector Velayos and Maj-Britt Franzén, I have no words to express how grateful I am for what they have done for me, they know what I mean ;). La Nena, because she is simply worth it. Carmen González, with her a coffe can last for hours :). Ángel Álvarez and Javier Macías, their example and unconditional support always pushes me forward.

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Chapter 1

Introduction

This Master's Thesis, carried out at CERN, is related to the development of CARIOCA, the front-end chip for the muon system of the LHCb experiment. CARIOCA (CERN And RIO Current-mode Amplifier) is an Amplifier-Shaper-Discriminator (ASD) circuit with baseline restoration (BLR) composed by 8 identical channels. It has been designed and is being developed at CERN in 0.25 μm radiation hard CMOS technology.

During the time elapsed between my arrival at CERN and the completion of this thesis three CARIOCA prototypes have been measured (CARIOCA6 to CARIOCA8) and four have been or will be submitted (CARIOCA7 to CARIOCA10). CARIOCA6 is the first prototype that contains the full ASD+BLR chain. It was fully functional but it did not meet all the specifications required by the system. Three extra design iterations have been done up to now in order to improve the performance of the circuit.

This chapter gives an overview of the framework within which the project is developed and the specifications the front-end electronics have to fulfill. Chapter 2 describes the topology of the chip and Chapter 3 shows the results of the measurements and simulations of CARIOCA8[1], compared with previous prototypes when relevant. This prototype was fully characterized.

1.1   CERN

CERN is the European Organization for Nuclear Research. Even though its name can lead to confusion, the nature of the research done at CERN is related to the study of interactions between particles, not with nuclear weapons.

CERN is the world's largest laboratory for Particle Physics. Sometimes it is referred to as the European Laboratory for Particle Physics because this name describes better the activity of the laboratory. It was founded in 1954 by 12 European States close to Geneva, Switzerland. Nowadays it is run by 20 European Member States and counts with the participation of Institutes and

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[1]The number after CARIOCA indicates the prototype number

Universities of some 30 non-Member States. Researchers from these institutions are allowed to use CERN's facilities through their collaborations, even though their countries are not full members of CERN. The joint effort of these nations has enabled the creation of a research center no individual country could have afforded both in terms of money and human resources[2].

1.2   The Large Hadron Collider Project

The Large Hadron Collider (LHC) will be a particle accelerator where two beams of protons will collide in a controlled way at energies never achieved before in particle physics experiments, 14 TeV[3]. Beams of heavy ions (lead nuclei) will be accelerated as well, colliding in this case with an energy of 1150 TeV. The conditions in which this collisions will take place will be very similar to those right after the Big Bang. This will allow scientists to perform a deeper analysis of the structure of matter.

The LHC is a circular accelerator with a length of 27 Km located at 100 m underground. It will reuse the tunnel excavated for the previous particle accelerator built at CERN: LEP (Large Electron Positron Collider). Smaller and older accelerators still running at CERN are used to generate and pre-accelerate the two proton beams that are injected into the LHC rings. Protons are grouped in bunches of $\sim 10^{11}$ protons that collide at the interaction points every 25 ns. Particle detectors are placed around these points.

In each interaction an average of 25 minimum-bias events is produced. These are "soft" events where the momentum transfer is small. The particles that result from this interactions have a final transverse momentum too small to be interesting. Rarely, a large momentum transfer interaction occurs producing an interesting event. this high p_T event will overlap with several minimum-bias events, this is the so called *pile-up*. Pile-up is a serious difficulty that has to be overcomed to succeed in the experiments. It has to be possible to discriminate between interesting and uninteresting events. This imposes tough constraints to the detectors, the readout electronics and the trigger system. The detectors and front-end electronics have to have a fast response, a small dead time, high granularity and radiation hardness. The trigger system has to distinguish between minimum-bias events and high momentum events in a very short time.

There are four large scale experiments located around the ring:

- ATLAS: A Toroidal LhcApparatuS. It is a general purpose $p - p$ experiment. It is conceived to be able to detect as many kinds of particles as possible. The energies at which LHC will run have never been achieved an a physics experiment up to now. Consequently, phenomena never seen before could arise during the life time of the project, making of the highest importance the capability of identifying as many processes as possible. It

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[2]See [6] for further information.
[3]1eV = 1.6 10^{-19} J

is the biggest experiment in terms of size with a length of 40 m, a radius of 10 m and a weight of 7000 tons.

- CMS: Compact Muon Solenoid. It is a multi-purpose $p - p$ experiment as well as ATLAS. Its dimensions are 20 m of length and 7 m of radius and it weights 14000 tons.

- LHCb: Large Hadron Collider beauty experiment. It is a $p - p$ experiment devoted to b-quark physics and CP violation.

- ALICE: A Large Ion Collider Experiment. It is a heavy ion experiment where lead nuclei will be collided at high energy density. In this conditions the formation of a new phase of the matter, the quark gluon plasma, is expected. The study of this plasma is the aim of the experiment.

The technical challenges building a machine as LHC involve are just amazing. Controlling the trajectory and the cross section of the proton beams require a magnetic field that grows with the energy of the beam particles. LHC will operate at B = 8.4 T. This is the maximum magnetic field that can be obtained with the only superconductive magnets that fulfill all the constraints of the design. This limits the energy of the proton beams to 14 TeV. There are approximately 8000 magnets in the ring of various types (dipoles, quadrupoles, etc.) that carry out different missions (focusing the beam, bending it, etc.). Some 1300 of them have to operate at 1.9 K, what makes of LHC the biggest cryogenic system in the world. Cooling at this temperature requires the use of superliquid helium.

The LHC project has also no precedent in terms of cost ($\sim$ 3500 MCHF), luminosity[4], size and complexity of the accelerator and experiments and human resources (more than 4000 physicists and engineers are involved in this project).

But why building such a complex machine? The Standard Model of Particles and Forces summarizes all the present knowledge about the fundamental constituents of matter and their interactions. To a certain extent, it is a good approximation to reality, but there are still many questions about the fundamental nature of matter the Standard Model cannot answer and predictions it makes that have not been demonstrated yet. Actually, the Standard Model is probably a low-energy approximation of a more general theory and only by looking at what happens at higher energies new theories can be proposed.

One of the most thrilling challenges of the LHC Project will be the detection of the Higgs boson, if it exists. According to the Higgs mechanism, the universe is filled up with a Higgs field. All particles would get their mass from the interaction with this field. Different kinds of interactions would produce different masses and that would explain why fundamental particles have a mass and why it is different for different particles. Other questions the LHC project will try to answer are related to the existence of supersymmetry (SUSY), the possibility of deconfining quarks in a quark-gluon plasma, CP violation and the origin of the

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[4]The luminosity $\mathcal{L}$ of a collider is $\mathcal{L} = \frac{N_i}{\sigma_i}$ where N_i is the number of events per second and σ_i the cross section of reaction i
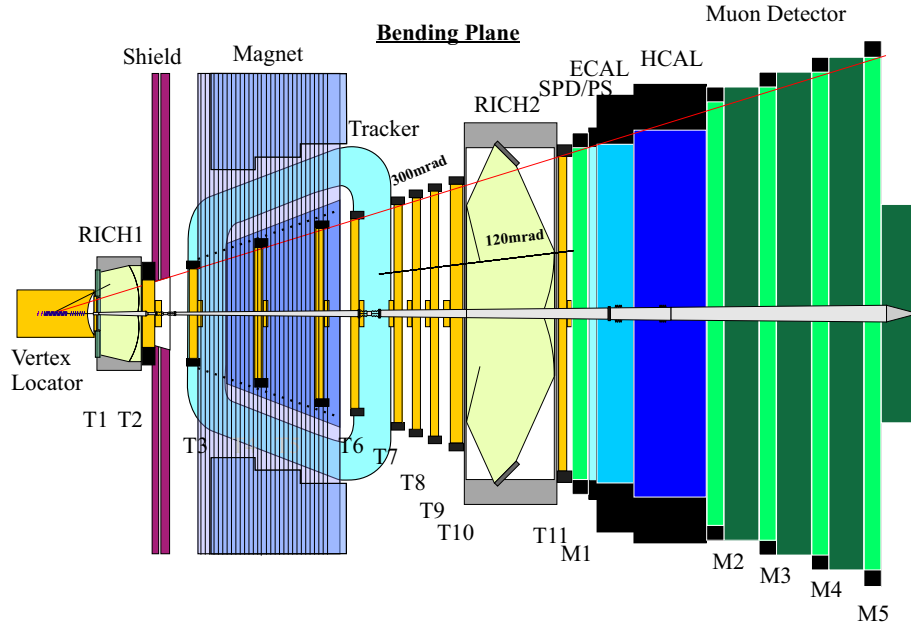
Figure 1.1: The LHCb detector seen from above (cut in the bending plane).

matter-antimatter imbalance[5], the discovery of new particles and many more that will for sure arise on the way[6].

1.3 LHCb

LHCb, shown if Figure 1.1, is the experiment that will study CP violation. But, what is CP violation and why is it so important? It is believed that after the Big Bang, matter and antimatter were created in equal amounts, but for some reason, nature favours matter over its counterpart, otherwise the world would not be as we know it. Understanding CP violation could be the key to find out why this is so.

There are three kinds of symmetries in particle interactions:

- C, charge conjugation. The application of C to a particle results in its anti-particle.

- P, parity. P gives the mirror image of a particle in all three coordinates.

- T, time reversal.

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[5]See Section 1.3 for more details about CP violation
[6]See [7, 8] for further information.

Some years ago, it was believed that symmetries were conserved, but experiments showed that C, P and CP are broken in some processes. CP is broken when there is a difference between the decay of a particle and the mirror image of the decay of its anti-particle. It is still believed that CPT is conserved, that is, that an antiparticle is indistinguishable from the mirror image of a particle moving backwards in time.

CP violation is necessary for the existence of an imbalance between matter and antimatter. The quark and antiquark transition probabilities state the probabilities they have of turning into different quarks and antiquarks. CP violation would only be possible if these probabilities were not equal, what would explain why nature prefers matter. The Standard Model does not quantify this probability matrix, leaving the door open for the existence of this phenomenon.

LHCb will measure these transition probabilities by studying the decays of B mesons. The degree of CP violation the Standard Model allows might not be enough to reflect reality. Therefore, after LHCb, the Standard Model will have a tough test to pass[7].

1.4 The Muon System of LHCb

Muons are present in many CP sensitive B decays. Therefore, muon identification is fundamental for the LHCb experiment. The muon system is the outermost of the detector since muons can go through all the stages that filter out all the other known particles. It consists of five muon stations placed in five planes parallel among themselves and orthogonal to the beam. They are named from M1 to M5, M1 being the inner one and M5 the outer one, meaning by inner the closer to the interaction point. Each station is divided into four different regions depending on their distance to the beam pipe. Each region has a different detector granularity because the number of events is higher in the cones that form a smaller angle from the collision point. Figure 1.1 shows the position of the muon system in the detector, Figure 1.2 gives a side view of the five muon stations and Figure 1.3 gives a front view of one quadrant of a muon station showing the placement of the regions.

The trigger logic is built so that all five stations have to fire to account for a detected muon. The total trigger efficiency has to be 95%, which means that every station has to have an efficiency of 99%. This extremely high efficiency is ensured by having a redundant system. Every station has two independent detector layers whose outputs are combined using the logical OR.

The background conditions are the most limiting factor for the efficiency of the system. The high rate at which the two proton beams are collided produces a huge quantity of particles. Only few of them are of interest among all the ones that produce some effect on the detectors. Reducing sensibly this enormous amount of data is essential for the experiment to succed, only the meaningful events should be recorded. The sooner the unimportant events are discarded the better. This is the job of the trigger system. LHCb uses a 3-levels trigger

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[7]See [9] for further information.

Muon Detector sideview
Arrangement of chambers in Y via overlapingProjectivity of chamber size from M1 to M5
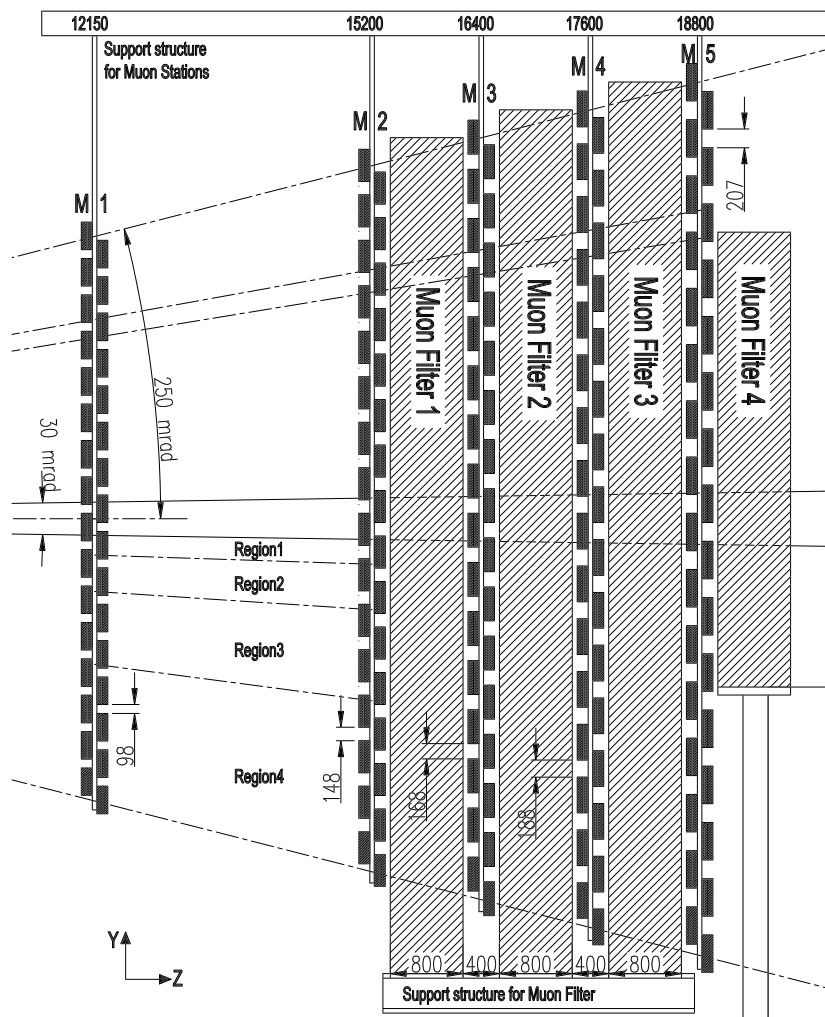
Figure 1.2: Side view of the LHCb muon system.
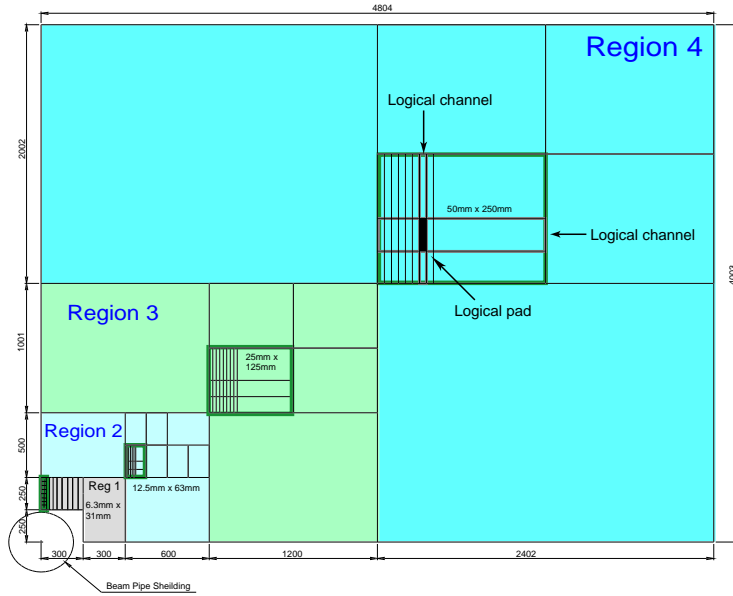
Figure 1.3: Front view of one quadrant of muon station M2 showing the disposition of the regions.

system. Level-0 and Level-1 use dedicated detector components for fast decisions whereas Level-2 and Level-3 use farms of commercial processors. The goal of this hierarchical trigger system is to reduce the rate at which events are read at Level-0, 40 MHz, to a storage rate of 200 Hz at the end of the trigger chain. The Level-0 muon trigger looks for muon tracks that define a straight line through the five muon stations that cross the interaction point discarding the low energy muons. The subsequent levels reduce the amount of data by selecting only the tracks containing a secondary vertex, which is a sign of the presence of a b particle, and in the end record only the data corresponding to certain kinds of interactions[8].

1.4.1 MWPC detectors

Multiwire Proportional Chambers have been adopted as detectors for the muon system. These particle detectors, created by the Nobel Prize winner Georges Charpak at CERN in 1968, are the most widely used detectors in particle physics experiments. They consist of a layer of parallel equidistant wires (anode) in between two cathode planes. One of these planes is divided into cathode pads and the other one is fully connected to ground. Figure 1.4 shows an schematic of a MWPC.

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[8]See [2] for further information.
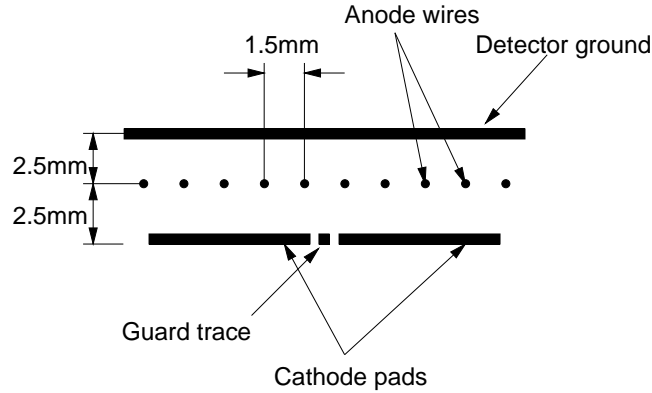
Figure 1.4: Schematic of a sensitive gap in a MWPC.

In the muon system of LHCb the pitch between the wires is 1.5 mm and the anode-cathode distance is 2.5 mm. Wires are grouped in pads of 4 to 42 wires depending on the granularity required by the station and the region. This granularity goes from 6 mm in region R1 of station M2 to 62 mm in region R2 of station M5. The required cathode pad size varies between 20×100 mm^2 in region R3 of station M1 and 62×77 mm^2 in region R2 of station M5.

The chambers are filled with a gas mixture, $Ar/CO_2/CF_4$ (40:50:10). The voltage difference between the anode and the cathode lies between 3 and 3.2 KV. This voltage drop in such a small space produces a high electric field in the gas gap. A muon crossing the chamber gap leaves in average 50 electrons that drift to the wires due to this electric field. As they get closer to the wires the increasing intensity of the electric field accelerates their motion giving them enough energy to create more electron-ion pairs resulting in an avalanche of charged particles. This avalanche of charged particles induces a negative signal on the wires and a positive signal with the same shape and about half of the magnitude on the cathode pads. The gas gain, $\sim 10^5$ in this case, defines the relation between the number of electrons produced by the primary ionization and the ones produced in the avalanche.

As it was pointed out before, in order to guarantee a station efficiency of more than 99% introducing some redundancy in the system is essential. Each chamber is composed of four sensitive gaps which are connected as two double gaps to two front end channels whose outputs are combined through an OR operation.

Depending on the region and the station the chambers have anode-wire readout (through decoupling capacitors), cathode pad readout or both. In total, the muon system requires 864 four gap chambers and about 80000 front-end channels.

The main characteristics of the MWPC used at the LHCb muon system are summarized in Table 1.1.

Parameter Name	Parameter Value
Gas Gap	5 mm
Wire spacing	1.5 mm
Wire diameter	30 μm
Operating voltage	3.0-3.2 kV
Number of gaps	4
Gas mixture	$Ar/CO_2/CF_4$ (40:50:10)
Primary ionization	~ 100 e^-/cm
Gas gain	$\sim 10^5$
Threshold	~ 3 fC
Charge/5 mm track	~ 0.8 pC

Table 1.1: Main characteristics of the MWPC used at the LHCb muon sytem.

1.4.2 Front-end Electronics Specifications

Both cathode and wire pads are readout. Therefore, both negative and positive polarities have to be handled by the front-end electronics. The average signal charge in the first 10 ns is 40 fC on the wire pads and 20 fC on the cathode pads. The dynamic range has to go up to 150 fC so as to guarantee a good tail cancellation for 95% of the signals. The signal has an ion tail with a time constant of $t_0 \approx 1.5$ ns. In order to suppress this tail maintaning a unipolar pulse shape so that the dead time is minimized, a double pole/zero filter network is recommended. The dead time is a critical factor of the system, due to the high input rate ($\sim$ 1 MHz) pileup is more likely to appear if the dead time is large. In the MWPC, the average arrival time of the last electron to the wire is about 30 ns. Therefore, the front-end should maintain the dead time under 50 ns in order to keep the efficiency high enough.

The input resistance should be smaller than 50Ω in order to maintain an acceptable level of cross talk from capacitive coupling between contiguous channels. The detector capacitance determines the noise level since it acts as a series noise source. Therefore, the front-end has to have a good noise performance through the detector capacitance range, which goes from 40 to 250 pF. The accumulated radiation dose in 10 LHC years will be about 1 MRad in station M1. This means that radiation hard electronic technologies have to be used. These specifications are summarized in Table 1.2.

Parameter Name	Parameter Value
Q_{ave} in 10 ns	40 fC
Input Polarity	Positive and Negative
Signal tail	$t_0 = 1.5$ ns
Detector capacitance	40-250 pF
Maximum signal rate	1 MHz
Maximum total dose	1 MRad
Decoupling capacitors	1 nF
Loading resistors	100 kΩ
Coupling	AC for wire signals
	DC for cathode signals
Peaking time at disc.	~ 10 ns
Equivalent noise charge	< 2fC for $C_{det} = 250$ pF
Linear range	150 fC
Input resistance	$< 50\Omega$
Shaping circuit	unipolar (2 pole/zero)
Average pulse width	< 50 ns
Baseline restorer	~ 1 μs response time

Table 1.2: Specifications for the front-end electronics of the muon system of LHCb.

Chapter 2

CARIOCA

As it was mentioned in Chapter 1 CARIOCA (CERN And RIO Current-mode Amplifier) is an Amplifier-Shaper-Discriminator (ASD) circuit with baseline restoration (BLR) composed by 8 identical channels.

This chapter describes briefly the blocks that form a CARIOCA channel. It is intended to give a general idea about the structure and working principle of this mixed signal circuit. Nevertheless, the level of detail will allow an easy understanding of the influence of the different subcircuits on certain figures of merit that will be presented in Chapter 3. For a more thorough description of the system refer to [1].

2.1   System Overview

Figure 2.1 shows the block diagram of a CARIOCA channel. This is a widely used topology for readout electronics of particle detectors. CARIOCA uses a current mode amplifier, what makes the response of the circuit very fast. This is important for this application since the arrival time of muons has to
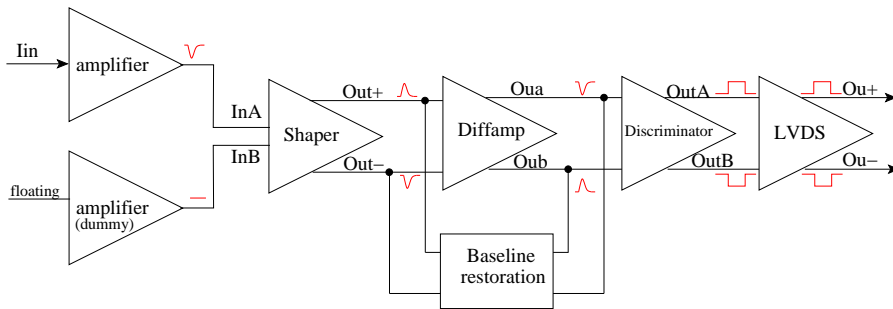

Figure 2.1: Block diagram of a CARIOCA channel.

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be determined with a precision better than 3 ns. The signal produced in the detector is a unipolar pulse with a very fast rising edge ($t_r < 1$ ns) and a long tail whose time response can be approximated by $\frac{1}{t+1.5ns}$ due to the ion mobility. This makes necessary the shaping of the signal to reduce the dead time as much as possible. The detector signal is first pre-amplified by this low gain fast amplifier, then goes through a unipolar shaping at the shaper and through a non-linear baseline restoration circuit that reduces the baseline fluctuations produced by the long tail of the input signal. This signal is presented to a discriminator circuit that depending on a threshold level set externally produces a pulse at the output when the input charge exceeds the threshold. The discriminator output is conditioned by an LVDS driver.

The signal produced at the MWPC is single ended. From the shaper input to the discriminator output the circuit is fully differential. The two input terminals of the shaper are connected to two identical preamplifiers. One of this amplifiers is connected to the MWPC output and the other one is connected to ground through a capacitor whose value is similar to the capacitance of a chamber pad. This pseudo-differential input scheme has some advantages over the single ended one, namely a better common mode rejection ratio. It has also disadvantages; with two amplifiers the differential noise figure is slightly worse.

2.2 Current Mode Amplifier

In the original conception of the circuit, there were two different amplifiers, one for each input polarity. As a result, there were two versions of the chip: the positive and the negative. In CARIOCA8 the two versions of the preamplifier were merged by using transmission gates to switch between the circuitry of each polarity. Thus, at present there is only one version of the chip whose polarity can be selected through a control signal.

The simplified schematic of both versions of the amplifier is shown in Figure 2.2. The input and intermediate stages are common for both amplifiers up to CARIOCA9. The input stage is a telescopic cascode amplifier. It is connected to a feedback circuit composed by a capacitor, C_{feed}, and a resistance. C_{feed} integrates the input charge and increases the stability of the amplifier acting as a compensation capacitor. The resistance of the feedback is not implemented with a resistor because of the high noise it would introduce in the system but with a set of transistors, N3 to N5. N3 acts as a voltage to current converter. This current is mirrored by N4 to the feedback transistor, N5 and to the output stage. The output stage consist of an NMOS transistor, N6, for the positive polarity channel. The equivalent current mirror of the negative polarity channel is made of PMOS transistors. Therefore, a second current mirror that uses n-devices is ued so that the output signal has the same polarity for both positive and negative amplifiers. Thus, the following blocks can be common for both polarities. The gain of the amplifier can be easily modified by changing the ratio between the W/L of the output current mirror.

Figure 2.3 shows the small signal equivalent of the simplified version of the

(a) Negative   (b) Positive
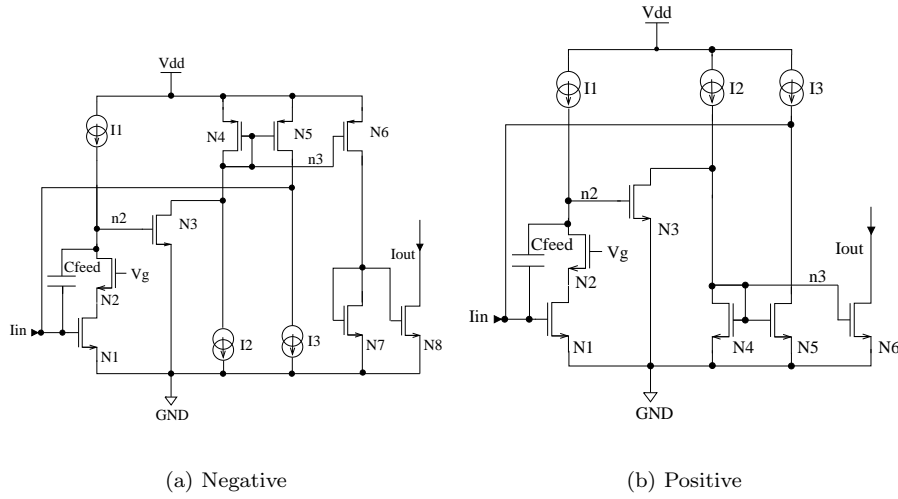
Figure 2.2: Simplified schematic of the negative and positive versions of the CARIOCA preamplifier.
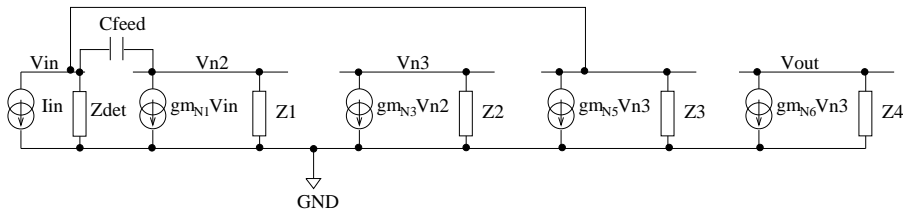
Figure 2.3: Small equivalent circuit of the simplified model of the preamplifier.

amplifier. The equations that describe this simplified model are:

$$I_{in} + \frac{V_{in}}{Z} + g_{mN5}V_{n3} - (V_{in} - V_{n2})C_{feed}s = 0 \tag{2.1}$$

$$g_{mN1}V_{in} + \frac{V_{n2}}{Z_1} - (V_{n2} - V_{in})C_{feed}s = 0 \tag{2.2}$$

$$g_{mN3}V_{n2} + \frac{V_{n3}}{Z_2} = 0 \tag{2.3}$$

$$g_{mN6}V_{n3} + \frac{V_{out}}{Z_{out}} = 0 \tag{2.4}$$

where $s = j\omega$, NX refers to transistor X, ny refers to node y, Z_z represents the total impedance at the current source node of I_z and $Z = Z_{det} \parallel Z_3 \approx Z_{det} \approx \frac{1}{sC_{det}}$.

The transfer function of the amplifier is obtained solving this set of equations:

$$\frac{I_{feed}}{I_{in}} = -\frac{(g_{mN1} + C_{feed}s)G}{g_{mN1}G - (C_{feed}(1 + g_{mN1}Z_1 - G) - C_{in})s - C_{feed}C_{in}Z_1s^2} \tag{2.5}$$

$$\frac{I_{out}}{I_{in}} = -\frac{\frac{g_{mN6}}{g_{mN3}}(g_{mN1} + C_{feed}s)G}{g_{mN1}G - (C_{feed}(1 + g_{mN1}Z_1 - G) - C_{in})s - C_{feed}C_{in}Z_1s^2} \tag{2.6}$$

where

$$G = g_{mN3}g_{mN5}Z_1Z_2 \tag{2.7}$$

The input impedance is:

$$Z_{in} = -\frac{1 - C_{feed}Z_1s}{g_{mN1}G - (C_{feed}(1 + g_{mN1}Z_1 - G) - C_{in})s - C_{feed}C_{in}Z_1s^2} \tag{2.8}$$

It is shown in Figure 2.4.

2.3   Shaper

The shaper used for CARIOCA is a one stage two poles two zeroes filter. Before entering the actual filter, the output currents coming from the amplifiers, I_{amp} and I_{dummy}, are converted to voltage by the circuit shown in Figure 2.5.

Figure 2.6 shows a simplified schematic of the shaper circuit. It consists of a differential amplifier in folded cascode configuration with a tail cancellation network formed by R_1, R_2, R_3, C_1 and C_2. The DC output voltage is set by the common mode voltage V_{CM} fixed to 1.27 V. The impedance of the tail cancellation network is:
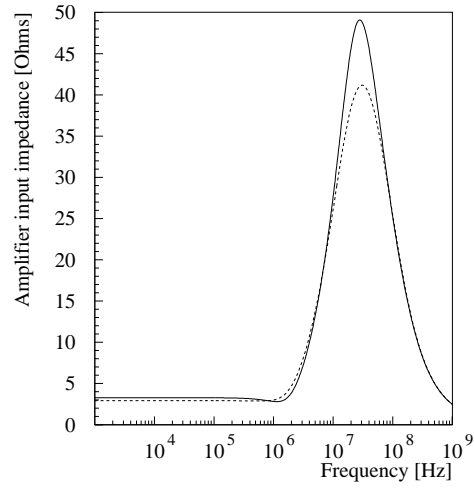
Figure 2.4: Input impedance of the preamplifier.
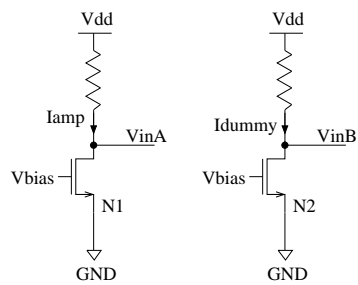
Figure 2.5: Current to voltage converter at the input of the shaper.
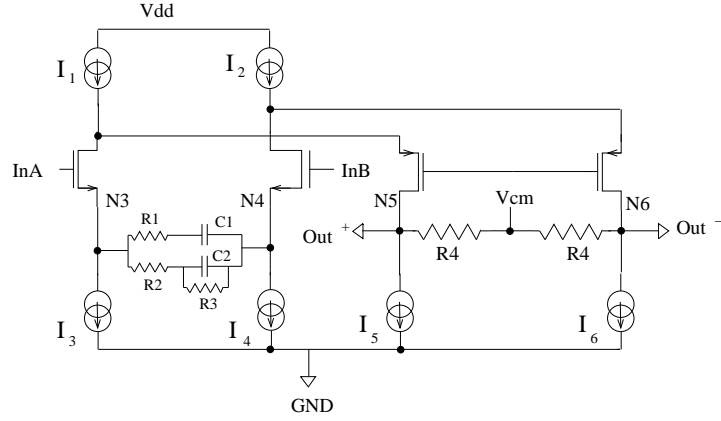
Figure 2.6: Simplified schematic of the shaper circuit.

$$Z = \frac{1 + (R_1 + R_2 + R_3)C_1 + R_3C_2)s + (R_1 + R_2R_3C_1C_2s^2}{(1 + R_1C_1s)(1 + \frac{C_2s}{\frac{1}{R_2} + \frac{1}{R_3}})} \qquad (2.9)$$

The frequency response of the shaper apart from constants is:

$$H(s) \propto \frac{1}{2 + g_m Z} \qquad (2.10)$$

Writing this expression as a function of the time constants of its poles and zeroes of the form:

$$H(s) \propto \frac{s + \frac{1}{\tau_1}}{s + \frac{1}{\tau_2}} \frac{s + \frac{1}{\tau_3}}{s + \frac{1}{\tau_4}} \qquad (2.11)$$

for $g_m = 2.15 m\mho$[1], $R_1 = 20K\Omega$, $R_2 = 2.7K\Omega$, $R_3 = 14K\Omega$, $C_1 = 2pF$ and $C_2 = 1.1pF$ yields

$$
\begin{aligned}
\tau_1 &= 8.73ns \\
\tau_2 &= 80.1ns \\
\tau_3 &= 3.14ns \\
\tau_4 &= 41.8ns
\end{aligned}
\qquad (2.12)
$$
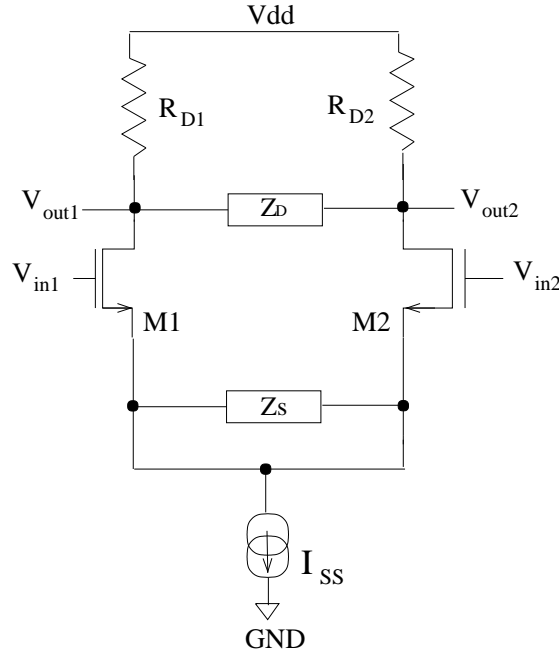
Figure 2.7: Simplified schematic of the differential amplifier.

2.4 Differential Amplifier

Figure 2.7 shows a simplified schematic of the differential amplifier. Its structure is very similar to the shaper. It basically consists of a differential pair with two passive networks. One of them, with impedance Z_S, is connected between the sources of the transistors that form the differential pair. The other, Z_D, is connected between the drains of these transistors. Thanks to these strategically placed passive networks, this differential amplifier not only amplifies, but also shapes the signal removing the tail added by the preamplifier.

Its frequency response apart from constants is:

$$H(s) \propto -\frac{4g_m}{2 + g_m Z_S}(R_D \parallel Z_D) \qquad (2.13)$$

where $g_m = g_{m1} = g_{m2}$, $R_D = R_{D1} = R_{D2}$, and the impedances Z_D and Z_S are:

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[1]This value is taken from simulation

$$Z_D = R_3 \tag{2.14}$$

$$Z_S = \frac{R_1(R_2 + \frac{1}{C_2 s})}{R_1 + R_2 + \frac{1}{C_2 s}} \tag{2.15}$$

The filtering doen by this differential amplifier corresponds to a one pole one zero filter. Expressing the transfer function of the differential amplifier as a function of the time constants associated with its pole and its zero:

$$H(s) \propto \frac{s + \frac{1}{\tau_1}}{s + \frac{1}{\tau_2}} \tag{2.16}$$

for CARIOCA8 $g_m = 2.359 m\mho^2$, $R_1 = 3.78 K\Omega$, $R_2 = 2.52 K\Omega$ and $C_2 = 1 pF$ produces:

$$\begin{aligned} \tau_1 &= 6.30 ns \\ \tau_2 &= 3.21 ns \end{aligned} \tag{2.17}$$

2.5 Baseline Restoration Circuit

The baseline voltage level of CARIOCA fluctuates due to the combination of DC coupling together with the long tails signals produce. This can lead to resolution problems due to pile-up. In order to minimize the drift these factors produce in the baseline voltage level a baseline restoration circuit (BLR) is included in CARIOCA.

This non-linear feedback circuit shown in Figure 2.8 is connected between the output and the input of the differential amplifier as shown in Figure 2.1. It consists of a chain of three differential amplifiers whose structure is similar to the one described in the previous section. In this case, no individual shaping is needed. Therefore, in the BLR Z_D[3] has been removed, and Z_S[4] consists of a resistor that acts only on the gain of the circuit.

For input signals smaller than the clipping voltage V_{clip} set by the first amplifier (BLR1), the BLR integrates and feeds back all the input signal. When V_{clip} is exceeded, BLR1 saturates keeping its output at V_{clip}. Thus, the BLR loses its linearity by integrating and feeding back the signal only up to V_{clip}. This non-linearity is introduced in order to keep the pulse as unipolar as possible after the BLR. Feeding back all the signal would produce a bipolar shape that would lead to a duplication of the dead time, which for large signals would make the system be out of specifications.

[2]This value is taken from simulation
[3]Z_D is the passive network that connected the drains of the input differential pair
[4]Z_S is the passive network that connected the sources of the input differential pair
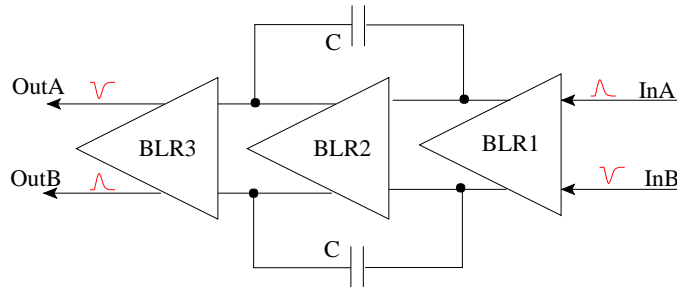
Figure 2.8: Block diagram of the baseline restoration circuit.

V_{clip} depends on the transconductance of the input transistors of BLR1 (g_{m1}) and the bias current of the amplifier (I_B) as:

$$V_{clip} = 2\frac{I_B}{g_{m1}} \tag{2.18}$$

The time constant of the BLR chain is given by:

$$\tau = \frac{C}{g_{m1}g_{m3}A_{diffamp}R_{sh}} \tag{2.19}$$

where g_{m1} and g_{m3} are the transconductances of the input transistors of BLR1 and BLR3 respectively, $A_{diffamp}$ is the gain of the differential amplifier and R_{sh} is the output impedance of the shaper that acts as the load of the BLR chain[5]. The longer the time constant, the smaller the impact of the BLR on the shape of the signal and the more stable the circuit. The original value of τ was 4.4 μs. It was reduced to 220 ns in order to decrease the pulse width of the output signal. The way this reduction was made is explained in Section 3.11

2.6 Discriminator

Figure 2.9 shows the schematic of the discriminator of CARIOCA. It is a high gain differential amplifier whose input differential pair is formed by transistors N1 and N2. In parallel with them, the differential pair formed by N3 and N4 sets the threshold that is controlled by their gate voltages V_{refA} and V_{refB}. A third differential pair is cross-coupled with them. It is formed by N5 and N6 and introduces hysteresis in the system, that is, a positive feedback that shifts the effective discriminator threshold and increases the speed of the output

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[5]It is actually the parallel of the output impedance of the shaper and the input impedance of the differential amplifier. The second is so big that its effect is negligible.

Figure 2.9: Schematic of the discriminator.

transitions. The amount of hysteresis is controlled by the bias current of this differential pair, I_{hyst}, called I_3 in Figure 2.9.

The output of the discriminator goes through an LVDS driver that adapts the signal level so that with a 100 Ω termination resistor the output signal has a peak to peak value of 300 mV and a DC level of 1.2 V.

2.6.1   DTV

The differential threshold fixed by V_{refA} and V_{refB} is obtained from a single threshold voltage that is set externally. The conversion between the single threshold voltage and the differential one is done by the differential threshold level (DTV) block.

Chapter 3

CARIOCA8 Characterization

This chapter shows the results of the measurements and simulations carried out for the eighth prototype of the CARIOCA ASIC. Comparison with previous prototypes is shown when significant improvements make it relevant. A brief description of the test setup and the software that was developed to control it is also included.

CARIOCA6 is the first prototype that contains the whole ASD+BLR chain with the LVDS driver at the output. It consists of two different chips, one for the positive polarity readout and one for the negative one. In CARIOCA7 only the version optimized for the positive polarity was implemented and the DTV block was added . CARIOCA8 is the first version in which the positive and the negative channels are merged. A control signal allows the selection of the polarity of the channel. A set of switches connects the subcircuits corresponding to the desired polarity disconnecting the ones of the opposite one. Channel 8 of this prototype contains six analog buffers that drive outside the chip the output of both preamplifiers and the two branches of the shaper output and the discriminator input. These buffers do not disturb significantly the behaviour of the channel because they only load slightly the circuits to which they are connected. According to simulation, they provide a scaled version of their input signal without modifying its shape.
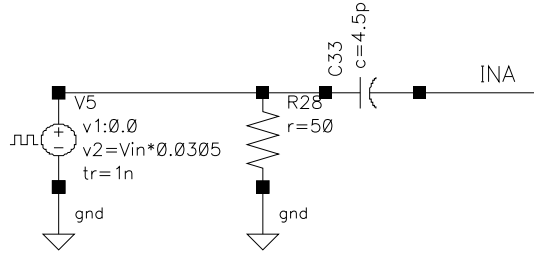
3.1   Simulation and Test Setup

All simulations were carried out with the Cadence Design Framework II (DFII) software[1] with IBM 0.25μm (cmos6sf) CMOS Library Design Kit[2].

As for the measurements, ten test boards containing two CARIOCA chips each have been tested. In one board one chip is sensitive to the positive polarity

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[1]Version IC 4.4.3

[2]Version 1.0.2 January 2001

Figure 3.1: Schematic of the δ injector.

and the other chip is sensitive to the negative one. Given that each CARIOCA chip contains eight channels, 80 channels per polarity can be tested. Channels 1 to 8 of the board correspond to channels 1 to 8 of the negative polarity chip and channels 9 to 16 of the board correspond to channels 1 to 8 of the positive polarity one. From now on, the channels will be named using the board number followed by the board channel number. Thus, channel 2.8 is channel 8 of board 2, therefore a negative channel and channel 7.10 is channel 10 of board 7, therefore a positive one.

The input is connected to a capacitor that emulates the detector. Several capacitance values are used in order to recreate the situation present in the different regions of the LHCb muon system. These values vary between 25 and 220 pF. The dummy input is connected to a capacitor of the same value in order to get a system as balanced as possible.

Two different signal injectors have been used: a δ injector and a $1/t$ injector. The δ injector shown in Figure 3.1 produces a current signal that is very similar to a delta when a voltage step goes through this network formed by a 50 Ω resistor and a 4.5 pF capacitor. This signal is used to characterize the delta response of the circuit. The charge of the signal that is connected to the input of the amplifier is:

$$Q_{in}(fC) = C_{inj}(pF) \cdot V_{in}(mV) = 4.5 \cdot V_{in}(mV) \qquad (3.1)$$

The $1/t$ injector, called this way just for convenience, produces actually a signal with a fast rising edge and a tail whose functional form is $1/(t + 1.5ns)$. This is a very good estimation of the signal a MWPC produces since the time constant of the ion tail is very close to this value. The RC network that transforms a voltage step into this $1/(t+1.5ns)$ current signal is shown in Figure 3.2. The input charge this injector produces is calibrated through measurement. This results are shown in Section 3.5.4.
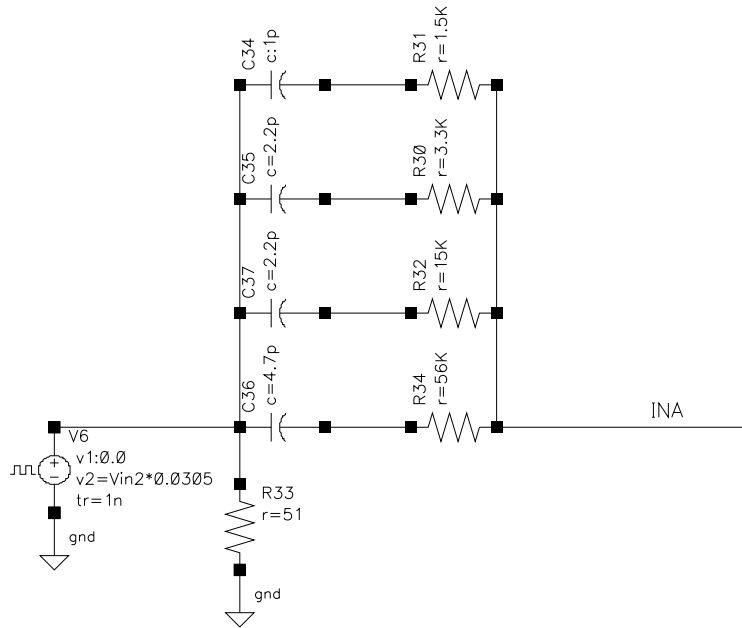
Figure 3.2: Schematic of the $1/(t + 1.5ns)$ injector.

In reality, an Agilent Technologies 81130A pulse generator[3] followed by a chain of attenuators is used to provide a voltage step of an appropriate amplitude. Some attenuation is needed for most of the measurements given the small charges muons induce on the MWPC[4]. The typical value for this attenuation is 30 dB. This attenuation value, combined with the output range of the pulse generator (from 50 mV to 2.5 V) provides a range of input charges that covers the values that will be found in the real system. In simulation, an ideal voltage source with a rise time of 1 ns is used.

The measurements that take little time and those whose automation is not worth the time and the effort have been done "by hand" using a LeCroy waverunner LT344 digital oscilloscope. Very time consuming measurements have been automated using a data acquisition system controlled by a software especially developed for this application based on LabVIEW[5]. Offset, s-curve and sensitivity measurements fall within this class. All of them involve intensive output signal counting. A block diagram of the test system is shown in Figure 3.3.

The output signal of CARIOCA has to be conditioned so that it can be read

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[3]See [15] for further information.
[4]See Section 1.4.2 for more detailed information.
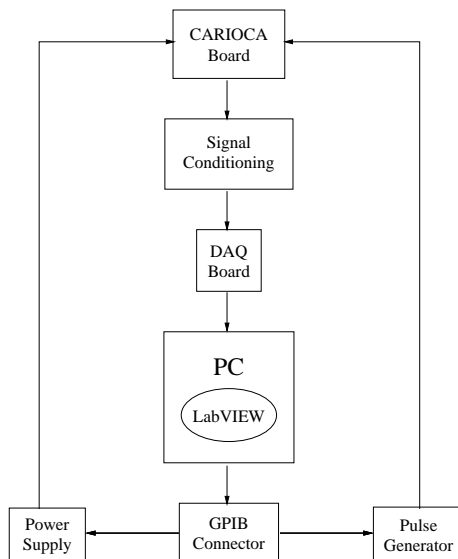[5]See [10, 11, 12].

Figure 3.3: Block diagram of the conditionining and data acquisition system implemented to test CARIOCA8

out by the DAQ board[6]. The signal conditioning part comprises the following blocks:

- LVDS[7]-ECL[8] converter from LNF.

- ECL-NIM[9] converter from Lecroy, model 4616.

- Discriminator from LRS, model 620CL with NIM input and output. This block provides a signal of a fixed pulse width of 25 ns. The minimum pulse width detectable by the DAQ board is 5 ns. Input charges exceeding only slightly the threshold can generate output signals with a pulse width so small that would make them undetectable by the DAQ system. Therefore, this discriminator ensures the detection of output signals with small pulse width.

- NIM-TTL[10] converter from LRS, model 688AL. This block is needed because the DAQ board has TTL input.

- SCB-68 from National Instruments[11]. This is a 68 pin shielded connector block that allows an easy connection to 68 pin National Instruments

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[6]See [13].
[7]Low Voltage Differential Signaling
[8]Emitter Coupled Logic
[9]Nuclear Instrumentation Methods
[10]Transistor-Transistor Logic
[11]See [14].

Parameter Name	Parameter Value
C_{det}	0 pF
I_{feed} positive	18 μA
I_{feed} negative	12 μA
I_{hyst}	6 μA
Injector	δ
Attenuation	42 dB

Table 3.1: Conditions of the analog sensitivities measurement.

C_{in} 0 pF	Measured Sensitivity (mV/fC)	Simulated Sensitivity (mV/fC)	Ratio
Neg Preamp	2.68	3.93	1.47
Pos Preamp	3.58	3.88	1.08
Neg Shaper	2.96	4.73	1.6
Pos Shaper	3.72	4.46	1.20
Neg BLR	3.32	5.54	1.67
Pos BLR	4.07	5.22	1.28

Table 3.2: Analog sensitivities of CARIOCA8.

devices like the DAQ board.

The DAQ board is the high speed counter timer for PCI bus PCI-6602 from National instruments. Obviously, it is connected to the PC through a PCI bus. This board contains 8 general purpose counters that are configured to perform simple event counting. A LabVIEW program controls their configuration and reads their values.

This LabVIEW program also controls the signals coming from the pulse generator and the power supply, a Hewlett Packard/Agilent Technologies E3631A triple output DC power supply[12]. The parameters that are selectable from the front panel of the virtual instrument are the period, width and amplitude of the pulsed signal and the amplitude of the DC threshold. This threshold comes from one of the outputs of the power supply. Another output sets the 2.5 V that power the circuit. This is controlled through the program in a transparent way to the user. Both the pulse generator and the power supply receive the SCPI[13] commands from the PC through a GPIB[14] cable.

3.2 Analog Sensitivities

The sensitivities of the channel up to the preamplifier output, the shaper output and the BLR output are measured with the oscilloscope connecting a probe to the analog outputs of channels 2.8 (negative) and 2.16 (positive). The conditions

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[12]See [16].
[13]Standard Commands for Programmable Instruments
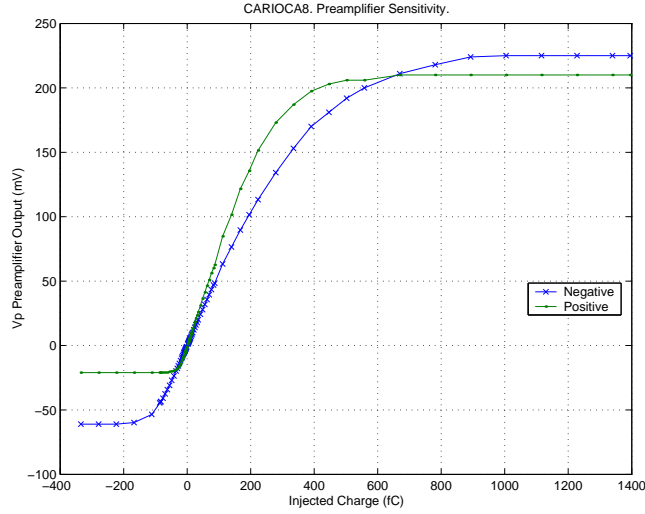[14]General Purpose Interface Bus

Figure 3.4: Measured sensitivity of the preamplifier for a δ input.

in which this measurement was done are shown in Table 3.1. Measurements and simulations are compared in Figures 3.4 to 3.7. Simulation shows that the analog buffer reduces the amplitude of the signals by a factor 5. It is assumed that this holds also in reality. The sensitivity values shown in Table 3.2 are calculated as the slopes of the output voltage vs. input charge curves considering only charges up to 200 fC to be sure of being in the linear range. The measured values shown in this table are already multiplied by five in order to give a more intuitive idea of the real gain of the subcircuits. On the contrary, the figures show the amplitudes after the buffer, that is, the real measurement.

Figure 3.4 shows that the linear range of the preamplifier goes up to nearly 300fC for signals of the correct polarity. This fulfills specifications since the preamplifier is the first block of the chain that saturates; remember from Section 1.4.2 that the dynamic range the circuit has to guarantee is 150fC. Having a large linear range is important since the tail cancellation stops being effective when the saturation region is reached. This leads to long dead times.

Sometimes, a channel finds at its input a signal whose polarity is opposite to the polarity for which the channel is optimized. This might happen due to crosstalk on the MWPC. It is, therefore, important that the wrong polarity behaviour of the channel keeps linear for a while. Thus, when a wrong polarity signal goes through a channel it will not saturate, what would make the dead time produced by this event extremely long. As for the linearity of the preamplifier when signals of the wrong polarity are injected into its input it goes up to 30fC for the positive channel and to 100fC for the negative channel. This range is enough to keep the dead time due to this phenomenon reasonable in most cases. Only 20% of a signal is induced in an opposite polarity channel in
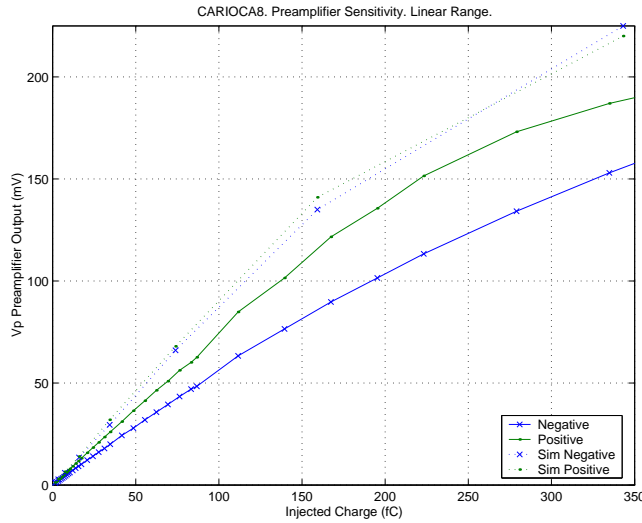
Figure 3.5: Sensitivity of the preamplifier for a δ input. Linear range.

the MWPC. 20% of the typical signal at the wire pads is around 8 fC and of the maximum expected signal for 95% of the cases is 30 fC. Hence, the linear range is more than enough for injected charges of both the correct and the wrong polarity.

Figure 3.5 zooms into the linear range of the preamplifier, this time showing simulation results too. The first thing that strikes when looking at this picture is the disagreement between simulation and measurements in the negative case. The slope of the positive polarity preamplifier is 8% smaller in reality than in simulation. In the negative polarity preamplifier this difference goes up to 47% as shown in Table 3.2.

Whereas this disagreement has an acceptable value for the positive channel, in the negative case this difference goes up to 47% as shown in Table 3.2. The first thing to look into in order to investigate this problem is the shape of the preamplifier output signal. This is discussed in Section 3.3. The following stages behave similarly for both channel polarities as it is shown in Figures 3.6 and 3.7 and Table 3.2. The preamplifier causes the difference between positive and negative channels.

The difference between simulation and measurements is partly explained by the use of an ideal pulse generator in simulation. Recording the signal produced by the actual pulse generator in the oscilloscope and using it in simulation instead of the ideal one produces simulation results that are within 10% of measurement results in all cases except for the negative preamplifier[15]. In order to investigate this disagreement for the negative preamplifier case, the first thing to look into is the shape of the signal. Results related to that are shown in the

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[15]This was shown by Nicolas Pelloux.
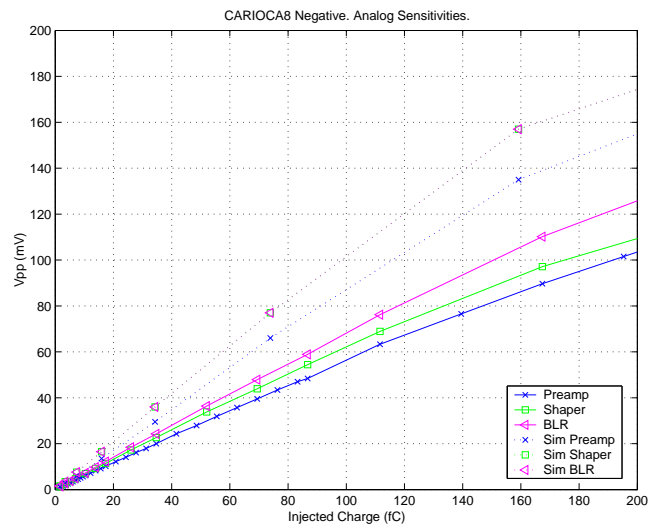
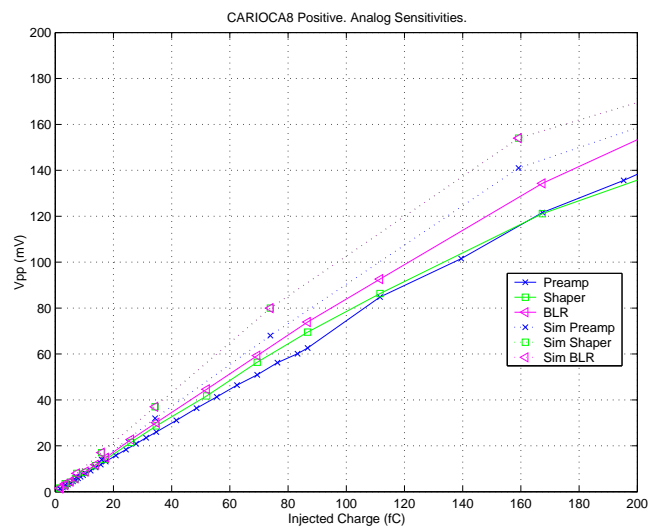Figure 3.6: Analog sensitivities for the negative polarity. Linear range.

Figure 3.7: Analog sensitivities for the positive polarity. Linear range.

Parameter Name	Parameter Value
C_{det}	0, 56, 100, 150 and 220 pF
I_{feed} positive	18 μA
I_{feed} negative	12 μA
I_{hyst}	6 μA
Injector	δ
Attenuation	30 dB
Injected charge	50 fC

Table 3.3: Conditions of the preamplifier output shape measurement.
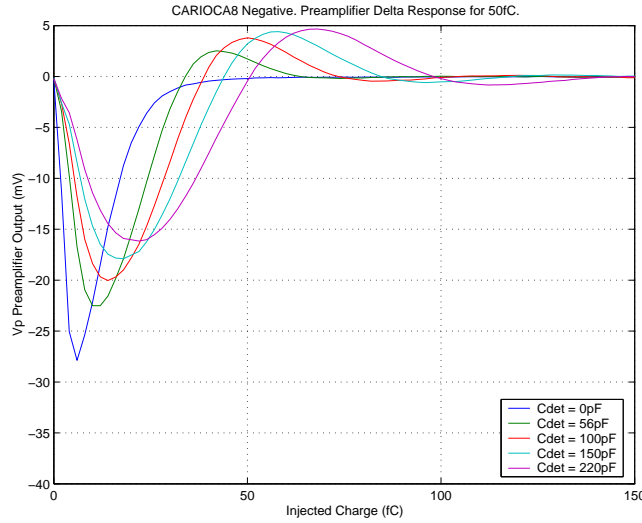
Figure 3.8: Measured shape of the negative preamplifier output for a δ input signal of 50 fC for different detector capacitances.

following section.

3.3 Preamplifier Output Shape

A δ signal of 50 fC is injected to the channels used in the previous section in the conditions shown in Table 3.3. The output of the preamplifier for different detector capacitance values is shown in Figure 3.8 for the negative case and in Figure 3.9 for the positive one. These curves have been recorded from the oscilloscope. They confirm the difference in gain between the positive and the negative versions of the preamplifier discussed in Section 3.2, even though they are designed to be identical. They also show the evolution of the signal shape with detector capacitance. Increasing the detector capacitance has an impact on both the gain and the pulse with, decreasing the first and increasing the last.
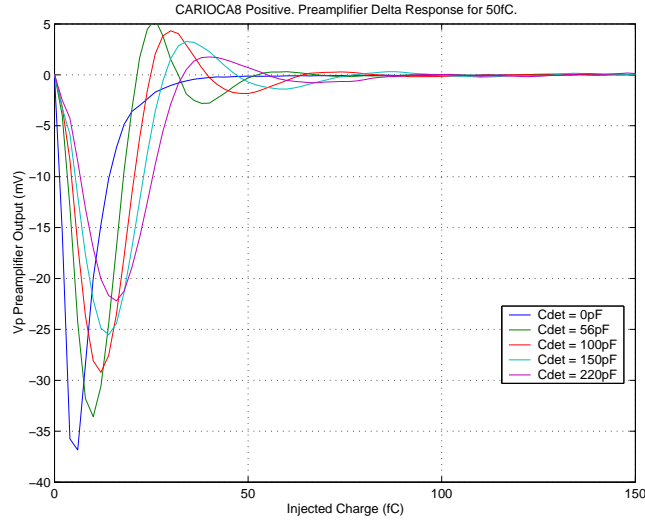
Figure 3.9: Measured shape of the positive preamplifier output for a δ input signal of 50 fC for different detector capacitances.

Note especially the difference in the rise time and the pulse width between the positive and the negative.

Figures 3.10 to 3.14 show the normalized values of the measured and simulated preamplifier output. The pulse shape is fairly well predicted for the positive circuit, but there is a large discrepancy between simulation and reality for the negative one. This normalized figures highlight the fact that the unexpected behaviour of the negative preamplifier is not only related to its sensitivity, as it was shown in Section 3.2, but mainly to its shape. The effects of this drift will have an impact mainly on the sensitivity of the full chain[16] and the pulse width of the output pulse[17]. The possible origin for this is the bad biasing of some transistors of the negative preamplifier that makes them work in regions that differ from their nominal working regions. This makes them very sensitive to process variations. Simulation has shown that this has an influence on the shape of the signal leaving the amplifier. In CARIOCA10 the schematic of the negative amplifier has been modified in order to solve the problem with the bias, what makes the circuit less sensitive to process variations. The test of CARIOCA10 will show whether this is the actual cause of the unexpected shape of the negative amplifier output.

Another important effect that is reflected in these figures is the small ringing the preamplifier output presents for both polarities. This ringing is dued to the association between the detector capacitance C_{det} and the input impedance of the amplifier Z_{in} determined by Equation 2.8 and shown in Figure 2.4. This in-

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[16]See Section 3.5
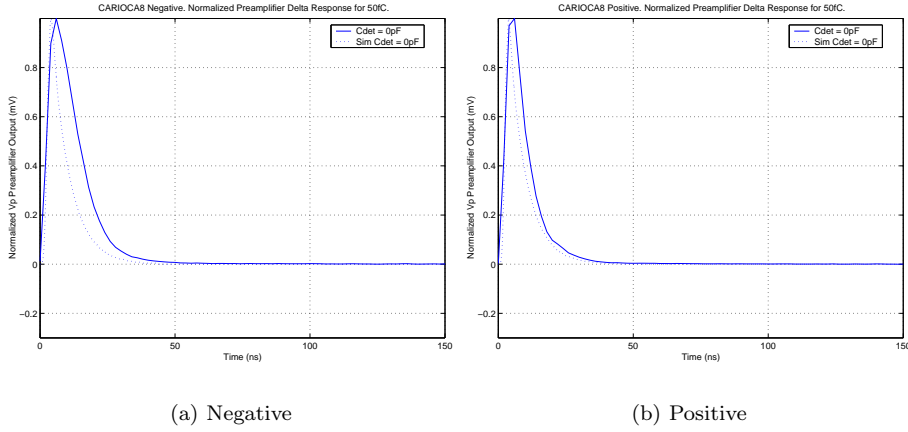[17]See Section 3.11

(a) Negative

(b) Positive

Figure 3.10: Normalized shape (solid line) and normalized simulated shape (dashed line) of the preamplifier output for a δ input signal of 50 fC for Cdet = 0 pF.
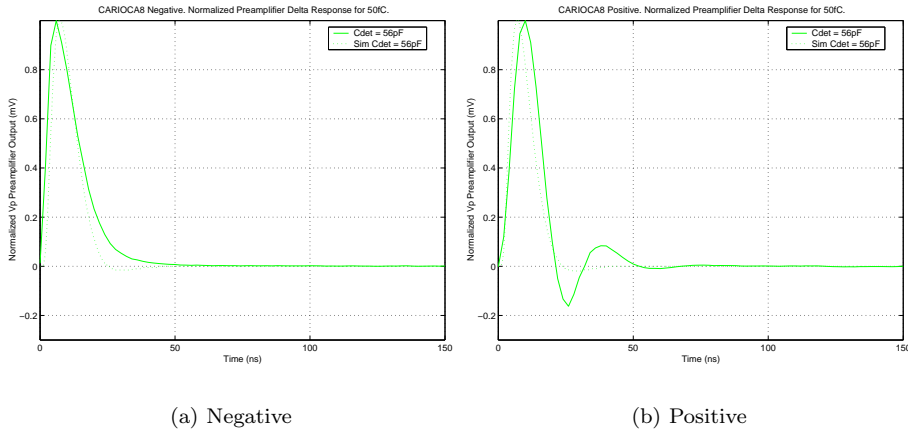

(a) Negative

(b) Positive

Figure 3.11: Normalized shape (solid line) and normalized simulated shape (dashed line) of the preamplifier output for a δ input signal of 50 fC for Cdet = 56 pF.
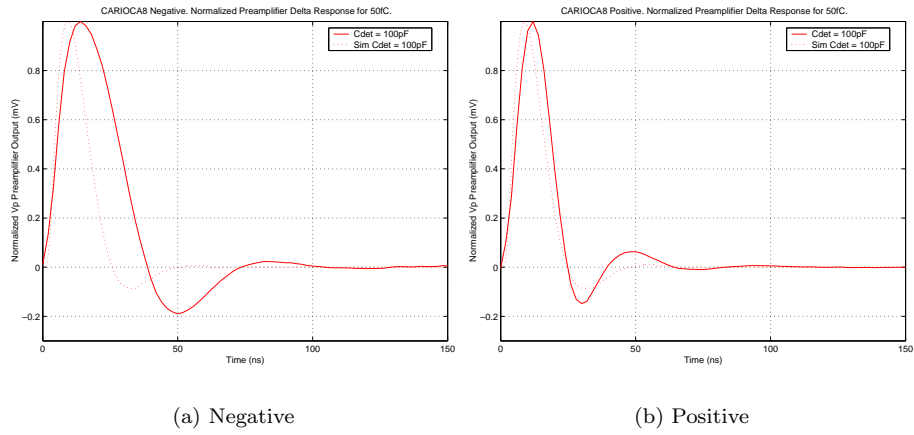
(a) Negative

(b) Positive

Figure 3.12: Normalized shape (solid line) and normalized simulated shape (dashed line) of the preamplifier output for a δ input signal of 50 fC for Cdet = 100 pF.

(a) Negative

(b) Positive

Figure 3.13: Normalized shape (solid line) and normalized simulated shape (dashed line) of the preamplifier output for a δ input signal of 50 fC for Cdet = 150 pF.
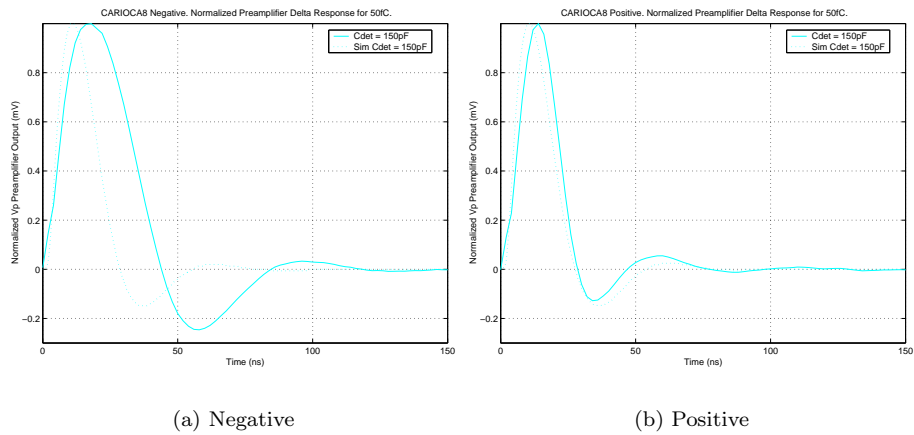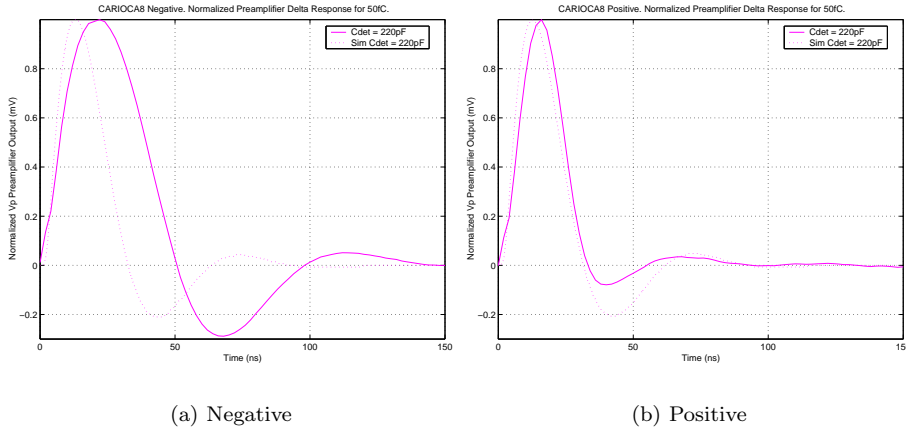
(a) Negative

(b) Positive

Figure 3.14: Normalized shape (solid line) and normalized simulated shape (dashed line) of the preamplifier output for a δ input signal of 50 fC for Cdet = 220 pF.

Parameter Name	Parameter Value
C_{det}	0 pF
I_{feed} positive	18 μA
I_{feed} negative	12 μA
I_{hyst}	6 μA

Table 3.4: Conditions of the threshold offset measurement.

put impedance makes the amplifier be equivalent to an RL circuit which together with the detector capacitance forms an RLC circuit. The input impedance has been changed for CARIOCA10 so that it is not equivalent to an LC circuit anymore.

3.4 Threshold Offset Variations

The nominal DTV threshold value that sets a differential threshold of 0mV is 800 mV. The actual value varies from channel to channel mainly due to process variations. It is calculated by sweeping V_{th} and looking at the V_{th} where the peak of the noise is located.

The threshold offset is measured in the conditions shown in Table 3.4 in all the 160 channels (8 channels/chip $\times$ 20 chips = 160 channels, 80 per polarity).

The distribution of the offset taking into account all the channels is shown in Figure 3.15. Its average and standard deviation are shown in Table 3.5. CARIOCA8 has one DTV block per chip. This allows setting the threshold
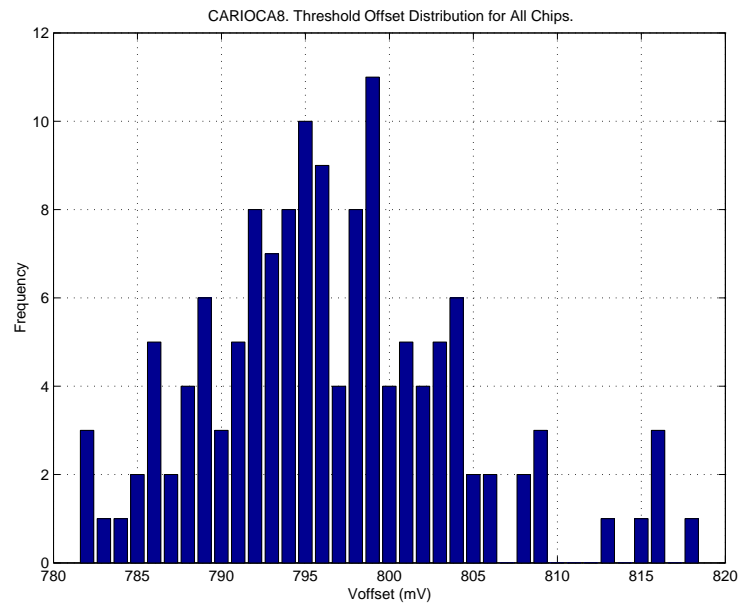
Figure 3.15: Histogram of the threshold offset distribution for 160 CARIOCA8 channels.
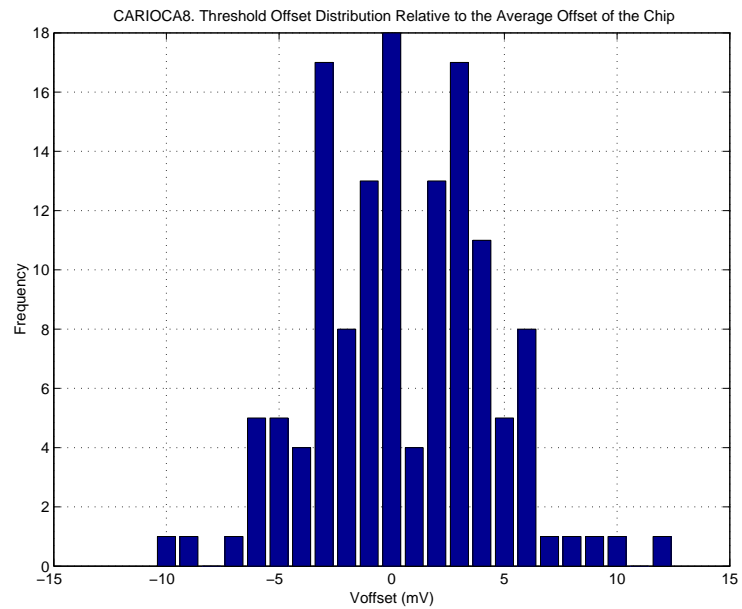

Figure 3.16: Histogram of the threshold offset distribution for 160 CARIOCA8 channels relative to the average offset of the chip they belong to.

V_{offset}	μ	σ
All Chips	796.92 mV	7.80 mV
Single Chip	799.94 mV	4.42 mV

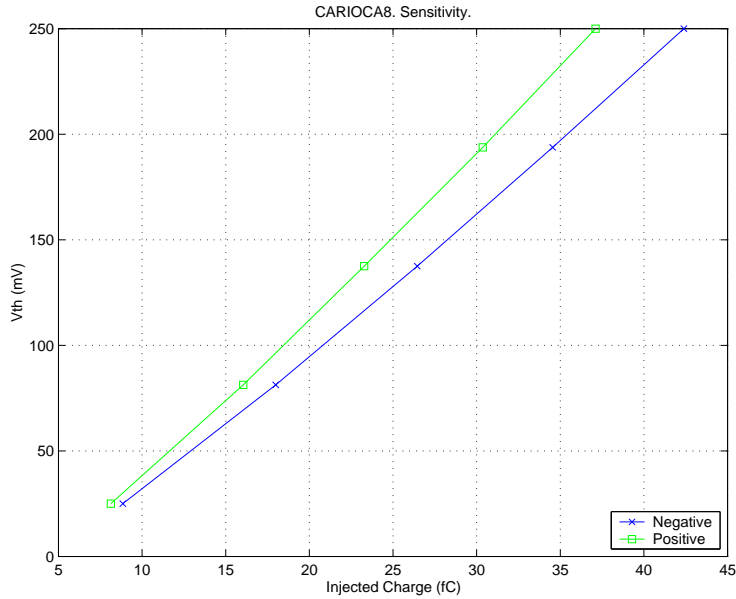Table 3.5: Threshold offset measurement results.

Figure 3.17: Measured sensitivity of channels 2.8 (negative) and 2.16 (positive).

voltage for each individual chip. Therefore, Figure 3.16 shows a more realistic scenario since it centers the offset value of each channel around the average offset of the chip it belongs to. The average and standard deviation of this distribution are shown as well in Table 3.5. This value fulfills the specifications, but it is close to the limit. Hence, the next prototype, CARIOCA9, will include one DTV block for each channel so that each threshold can be set individually.

3.5 Sensitivity of the Full Chain

Figure 3.17 shows the sensitivity of channels 2.8 (negative) and 2.16 (positive) measured in the conditions shown in Table 3.6. These are typical sensitivity curves[18].

In reality the sensitivity of the full chain is smaller for the negative channel than for the positive one whereas in simulation both of them are very similar. This is expectable since the actual gain of the negative preamplifier is smaller

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[18]Statistics will confirm this statement in Section 3.5.3.

Parameter Name	Parameter Value
C_{det}	0 pF
I_{feed} positive	18 μA
I_{feed} negative	12 μA
I_{hyst}	6 μA
Injector	δ
Attenuation	30 dB

Table 3.6: Conditions of the sensitivity measurement.

than the gain of the positive one and their shapes are different, effects that are not seen in simulation[19]. Both positive and negative channels show a smaller sensitivity in reality than in simulation.

The sensitivity is linear in this range, which is a good characteristic of the circuit. However, a threshold voltage of 0 mV does not correspond to 0 fC input charge. This makes the minimum detectable charge different to zero. This effect is introduced by the discriminator, since as it was shown in Section 3.2 the sensitivity curves up to its input cross the origin. The smaller the minimum detectable charge is the better. In reality it is not possible to lower down the threshold voltage much more than what is shown in these curves. The reason is that for low threshold values signal and noise levels become comparable. This produces a count rate at the output that is more related to the noise than to the sensitivity of the system. The abscissa of the point where the linear extrapolation of the sensitivity curve cuts the horizontal axis is considered to be the minimum detectable charge. In simulation, the curve is linear down to approximately 3 fC and then it starts bending until it crosses the origin. Hence, this is an intrinsic characteristic of the circuit. The sensitivity curve will not cross the origin in its linear range. Even so, the extrapolated minimum detectable charge should be reduced as much as possible in order to increase the performance. Increasing the gain up to the discriminator input would both increase the slope of the full chain sensitivity and reduce the minimum detectable charge. CARIOCA10 will include this modification. The effect of external parameters such as the hysteresis current and the detector capacitance as well as the uniformity of the sensitivity along the different channels is discussed in the following sections. Every time a sensitivity curve is measured the offset of the threshold voltage is taken into account so that variations in this value have no effect on the sensitivity measurement.

3.5.1   Variation of the Sensitivity with the Hysteresis

The variation of the sensitivity with the hysteresis current fed into CARIOCA is shown in Figure 3.18 and Table 3.8. The measurement was done for channels 2.8 (negative) and 2.16 (positive) on the conditions of Table 3.7. Hysteresis worsens slightly the slope of the sensitivity and the minimum detectable charge.

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[19]See Section 3.2.

Parameter Name	Parameter Value
C_{det}	0 pF
I_{feed} positive	18 μA
I_{feed} negative	12 μA
I_{hyst}	0 and 6 μA
Injector	δ
Attenuation	30 dB

Table 3.7: Conditions of the variation of the sensitivity with the hysteresis current measurent

Parameter	Polarity	$I_{Hyst} = 0\ \mu A$	$I_{Hyst} = 6\ \mu A$
Slope of the Sensitivity	Negative	6.75 mV/fC	6.71 mV/fC
	Positive	7.87 mv/fC	7.77 mV/fC
Minimum Detectable Charge	Negative	4.65 fC	5.58 fC
	Positive	4.48 fC	5.3 fC

Table 3.8: Variation of the measured sensitivity with the hysteresis current.

The importance of this effect is negligible, especially considering the advantages a moderate hysteresis has in terms of noise immunity.
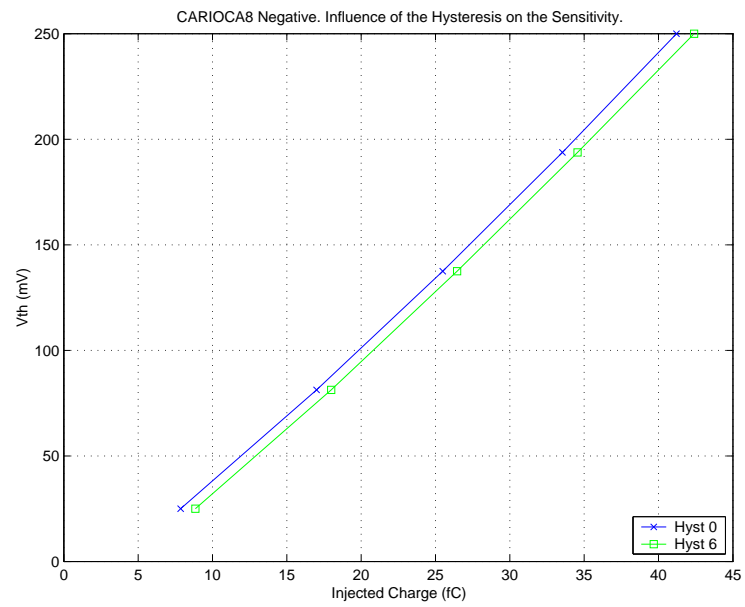
3.5.2   Variation of the Sensitivity with the Detector Capacitance

The evolution of the sensitivity curves for increasing detector capacitance values can be seen in Figures 3.19 to 3.21. Both positive and negative channels become more sensitive to the noise for large capacitance values as Section 3.6 will show. This increases the minimum threshold voltage needed to be able to distinguish noise from signal. As the capacitance value grows the sensitivity decreases and the minimum detectable charge increases. This can be clearly observed in Figures 3.20 and 3.21. These measurements were done on channels 2.8 (negative) and 2.16 (positive) under the conditions shown in Table 3.9 for an unbalanced system, i.e. only the preamplifier input is connected to C_{det}, the input of the dummy preamplifier is left open. This measurement was not done with a balanced input for the reasons explained in Section 3.12

3.5.3   Uniformity of the Sensitivity

This section presents the statistics done around the distribution of the slopes of the sensitivity curves of some 60 channels per polarity. Information about the minimum detectable charge is also included. Table 3.10 shows the conditions in which the measurements were done. Figures 3.22 to 3.24 and Tables 3.11 and 3.12 show the results.

The spread of the slope of the sensitivity is nearly a factor 2 larger for the negative channel than for the positive one. Its mean value is better predicted
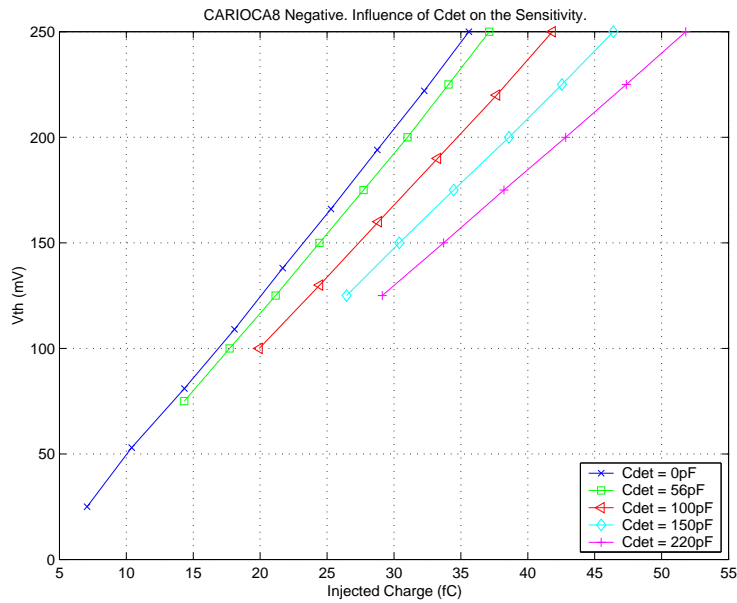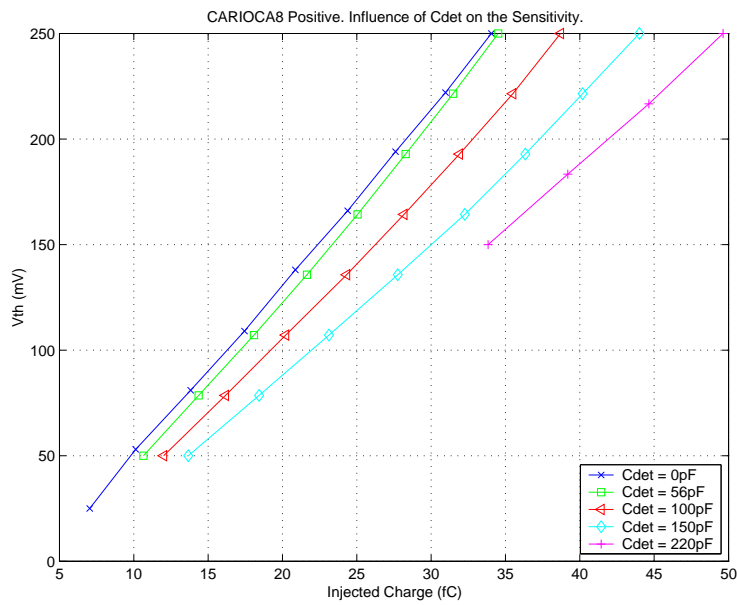
(a) Negative
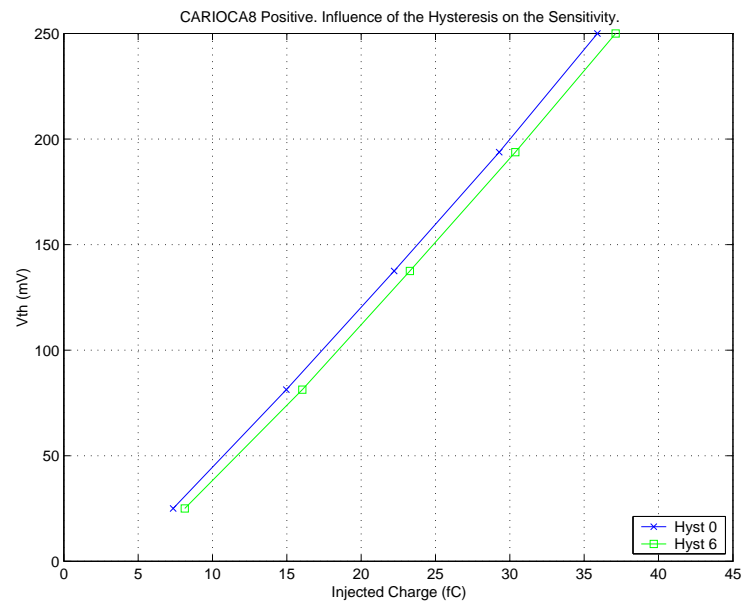
(b) Positive

Figure 3.18: Variation of the sensitivity with the hysteresis current for channels 2.8 (negative) and 2.16 (positive).

(a) Negative

(b) Positive

Figure 3.19: Variation of the measured sensitivity with the detector capacitance for channels 2.8 (negative) and 2.16 (positive).

Parameter Name	Parameter Value
C_{det}	0, 56, 100, 150 and 220 pF
I_{feed} positive	18 μA
I_{feed} negative	12 μA
I_{hyst}	6 μA
Injector	δ
Attenuation	30 dB

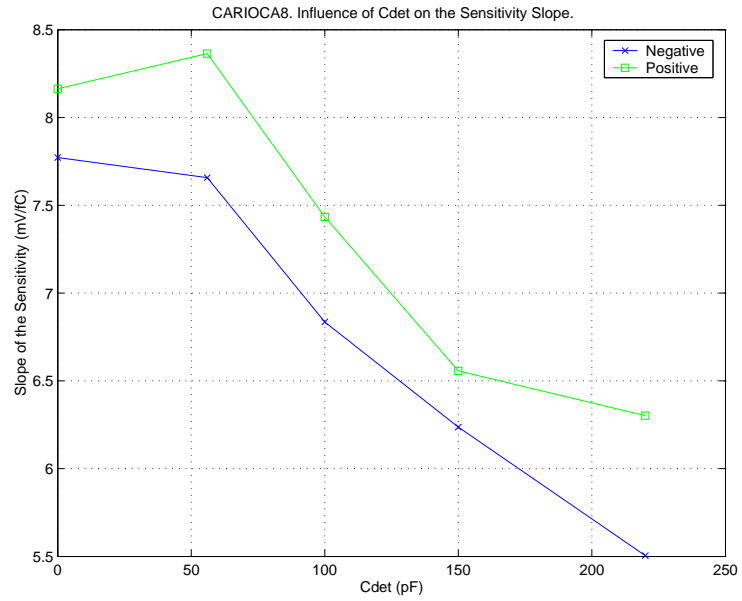Table 3.9: Conditions of the variation of the sensitivity with the detector capacitance measurent.

Figure 3.20: Influence of the detector capacitance on the slope of the sensitivity.

Parameter Name	Parameter Value
C_{det}	0 pF
I_{feed} positive	18 μA
I_{feed} negative	12 μA
I_{hyst}	6 μA
Injector	δ
Attenuation	30 dB

Table 3.10: Conditions of the uniformity of the sensitivity measurent.

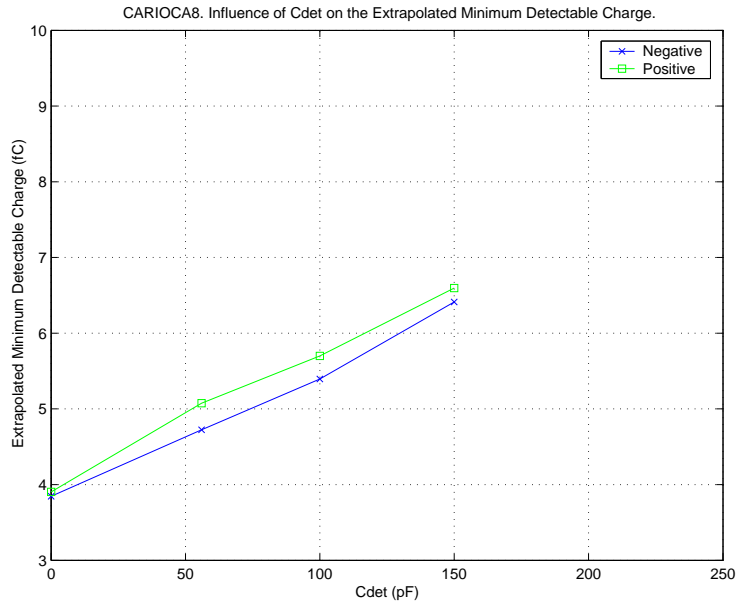Figure 3.21: Influence of the detector capacitance on the minimum detectable charge.

Parameter	Negative (Sim)	Positive (Sim)
μ Slope	7.70 mV/fC (10.63)	8.21 mV/fC (10.78)
σ Slope	0.32 mV/fC	0.18 mV/fC

Table 3.11: Average and standard deviation of the slope of the sensitivity.

for the positive channel. As for the minimum detectable charge, both types of channels have approximately the same value with the same spread.

3.5.4 Charge Injected by the 1/t Injector

The charge injected by the 1/t injector is calibrated measuring two sensitivity curves. The first curve plots the sensitivity of a channel in mV/fC for the δ injector, i.e. the vertical axis corresponds to the threshold voltage and the horizontal axis to the injected charge. The second curve plots the sensitivity of the same channel in mV/mV for the 1/t injector, i.e. the vertical axis corresponds to the threshold voltage and the horizontal axis to the voltage at the input of the injector. The combination of these two plots results in the curve shown in Figure 3.25, where the relation between the voltage at the input of the injector and the charge at its output is established and equals 2.6 fC/mV. Obviously, this value is the same for both polarities because it only depends on the passive network shown in Figure 3.2.
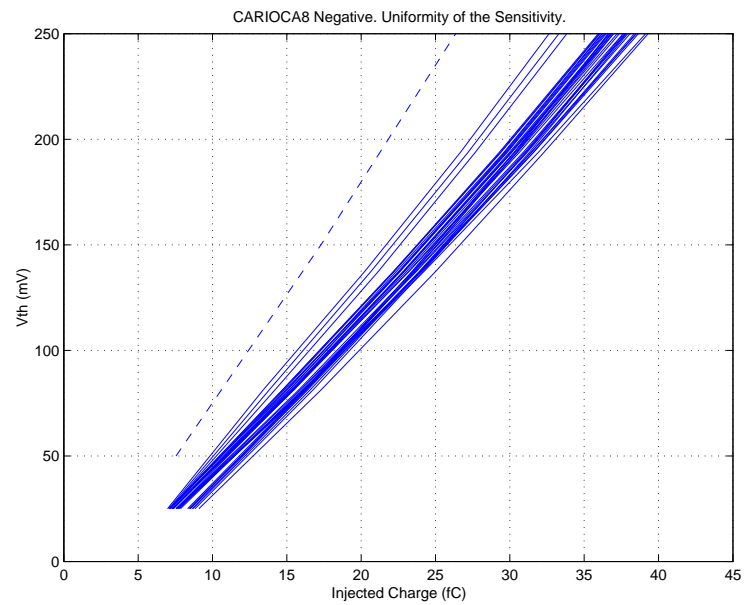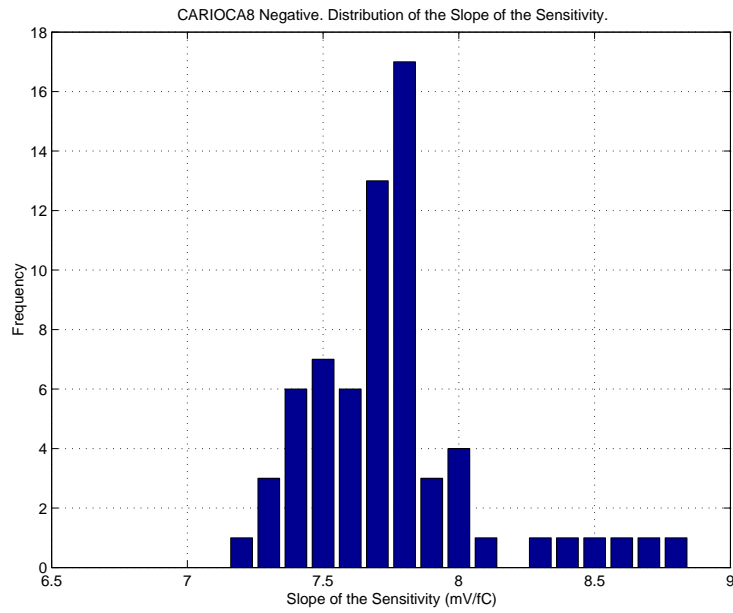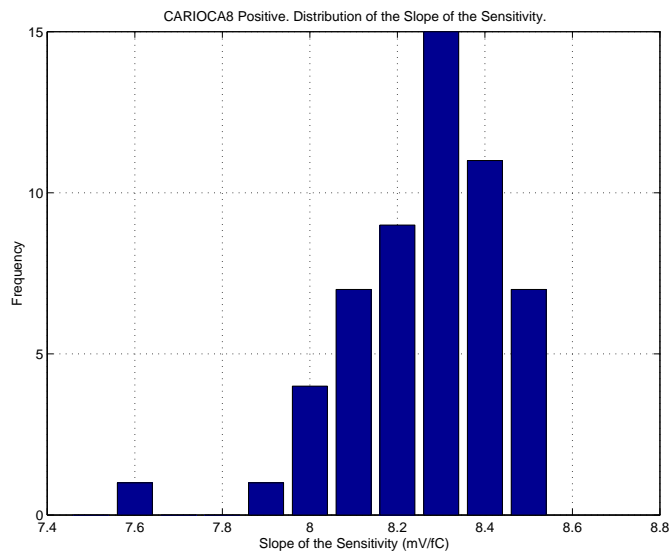
(a) Negative
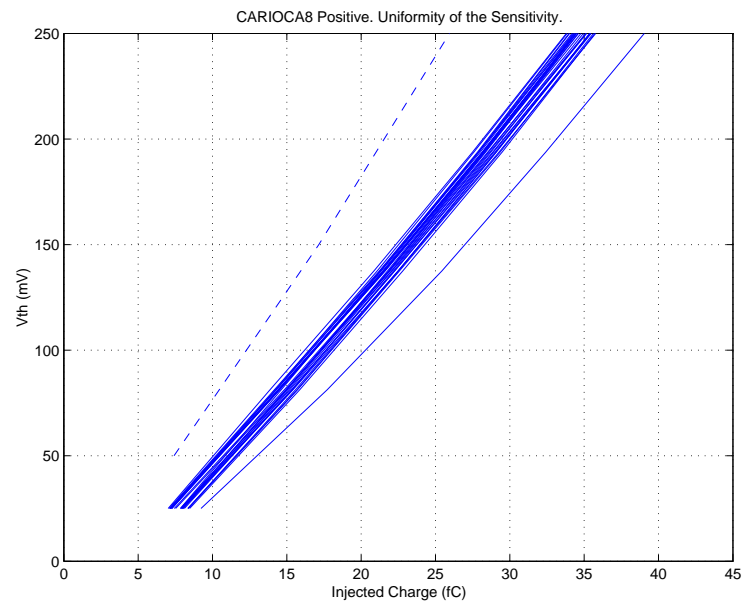
(b) Positive

Figure 3.22: Uniformity of the sensitivity. The solid lines correspond to the measurement results and the dashed line to the simulation.
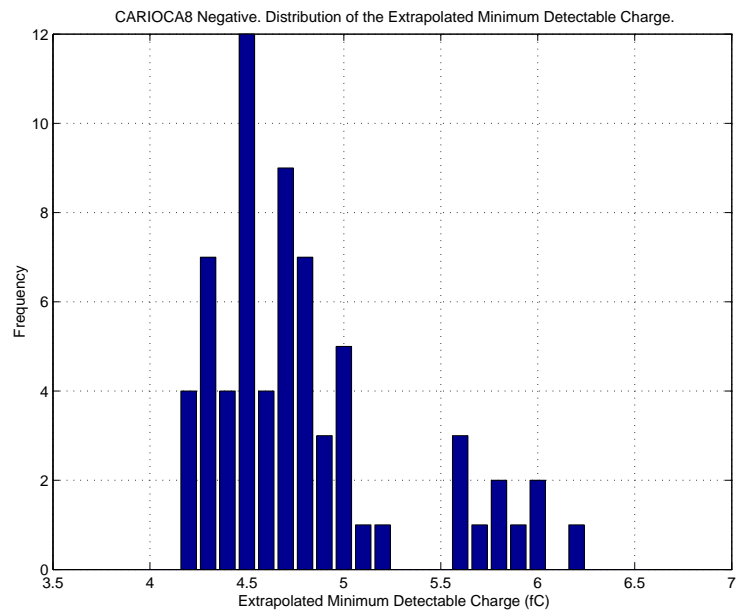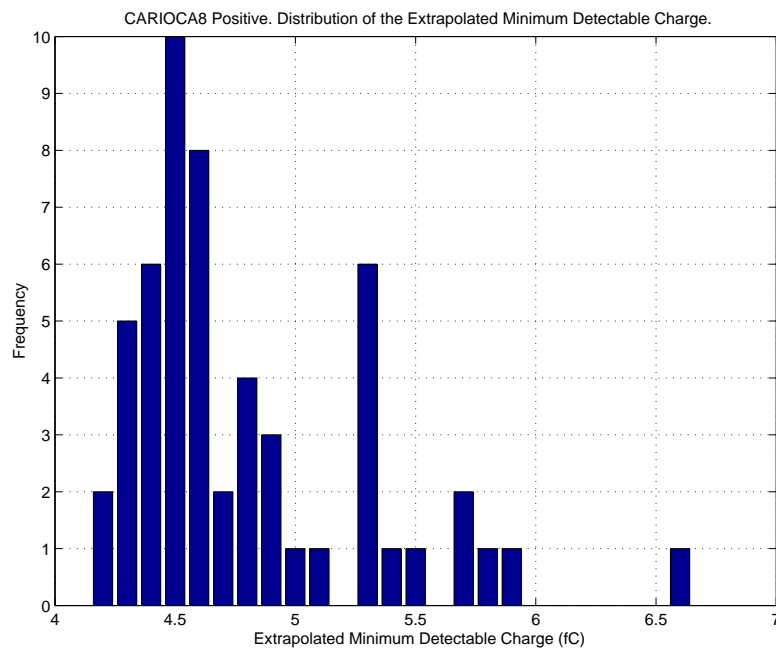
(a) Negative

(b) Positive

Figure 3.23: Distribution of the slope of the sensitivity.

(a) Negative

(b) Positive

Figure 3.24: Distribution of the extrapolated minimum detectable charge.

Parameter	Negative (Sim)	Positive (Sim)
μ Q_{min}	4.74 fC (2.96)	4.74fC (2.93)
σ Q_{min}	0.50 fC	0.50fC

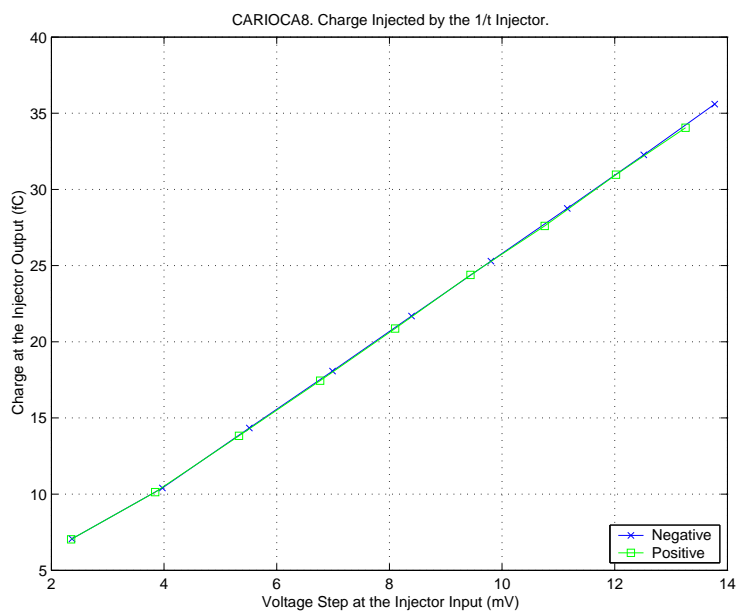Table 3.12: Average and standard deviation of the extrapolated minimum detectable charge.

Figure 3.25: Charge at the output of the 1/t injector.

Parameter Name	Parameter Value
C_{det}	0, 56, 100, 150 and 220 pF
I_{feed} positive	18 μA
I_{feed} negative	12 μA
I_{hyst}	6 μA
Injector	δ
Attenuation	30 dB

Table 3.13: Conditions of the variation of the noise with the detector capacitance measurent.

3.6 Variation of the Noise with the Detector Capacitance

The variation of the noise with the detector capacitance is shown in Figure 3.26. This measurement was done in the conditions of Table 3.13 for channels 2.8 (negative) and 2.16 (positive) for an unbalanced system, i.e. only the preamplifier input is connected to C_{det}, the input of the dummy preamplifier is left open. This measurement was not done with a balanced input for the reasons explained in Section 3.12.

For the negative polarity channel the noise equals:

$$2460 + 50e^-/pF \tag{3.2}$$

and for the positive

$$2157 + 50e^-/pF \tag{3.3}$$

The noise measured for CARIOCA6 with a balanced system is:

$$2600 + 45e^-/pF \tag{3.4}$$

for the negative and

$$2400 + 45e^-/pF \tag{3.5}$$

for the positive. Even adding the dummy capacitor, which acts as a noise source, leads to a lower noise level because the common mode noise is rejected.

3.7 Pulse Width

The pulse width of the output signal of CARIOCA8 for a 7 fC threshold is shown in Figure 3.27 for input signals of up to 300 fC and in Figure 3.28 for input signals
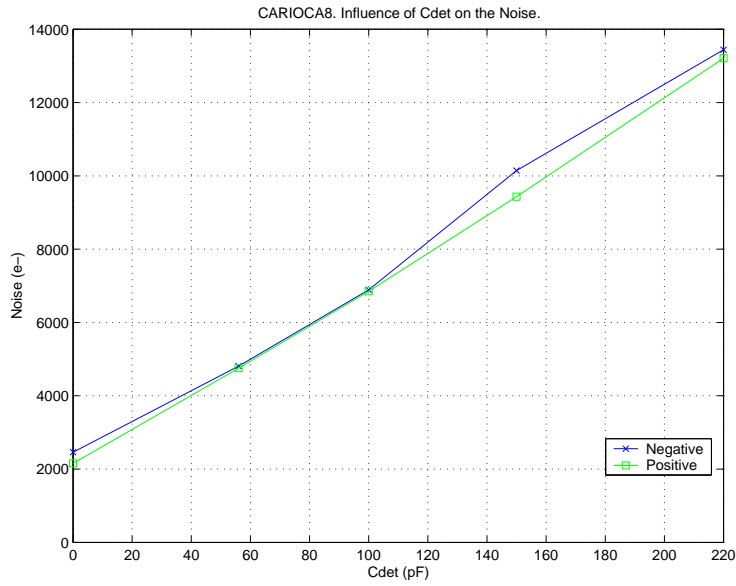
Figure 3.26: Variation of the measured noise with the detector capacitance for channels 2.8 (negative) and 2.16 (positive).

of up to 6 pC. The measurements were done in channels 8 and 16 of CARIOCA7 board number 9 where CARIOCA7 was substituted by CARIOCA8[20] in the conditions shown in Table 3.14.

The pulse width for charges up to 300 fC remains under 55 ns for the positive channel and under 65 ns for the negative one. This is around 30% better than the pulse width of CARIOCA6 as shown in Figure 3.29. The problem with the abrupt increase of pulse width of the positive polarity channel at 175 fC injected charge has been solved. This improvement in the pulse width characteristic of the circuit is dued to a reduction in the BLR time constant done in the way

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[20]This was done in order to gain time for the tests until the boards of CARIOCA8 were ready. Both boards are very similar, this should not have any influence on the result.

Parameter Name	Parameter Value
C_{det}	0 pF
I_{feed} positive	18 μA
I_{feed} negative	12 μA
I_{hyst}	6 μA
Injector	1/t
Attenuation	30 and 18dB

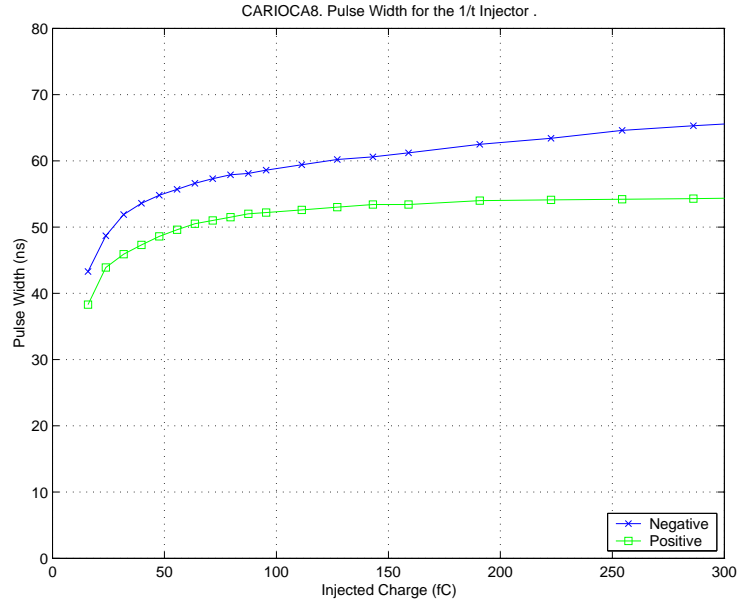Table 3.14: Conditions of the pulse width measurent.

Figure 3.27: Pulse width measurements for an input charge up to 300 fC.

described in Section 3.7.1. Nevertheless, this pulse width is still too high for the given specifications. In order to reduce it the shaping of the signal will be changed in CARIOCA10.

Figure 3.28 shows the pulse width measurements for charges up to 6 pC. In the unlikely case of having such a big input charge, the dead time would remain under 800 ns in any case. This is a very good characteristic of the circuit.

3.7.1   Pulse Width Reduction through the BLR

Reducing the time constant of the BLR, that is, making it faster, reduces the width of the pulse that the discriminator finds at its input. This obviously leads to a reduction in the output pulse width. Up to CARIOCA7 $\tau \simeq 4.4 \mu s$ and a value around 200 ns is desired for CARIOCA8. Remember from Section 2.5 that:

$$\tau = \frac{C}{g_{m1} g_{m3} A_{diffamp} R_{sh}} \tag{3.6}$$

where g_{m1} and g_{m3} are the transconductances of M1_{BLR1}, M2_{BLR1}, M1_{BLR3} and M2_{BLR3}, that is, the input transistors of BLR1 and BLR3, $A_{diffamp}$ is the gain of the differential amplifier and R_{sh} is the output impedance of the shaper that acts as the load of the BLR chain.
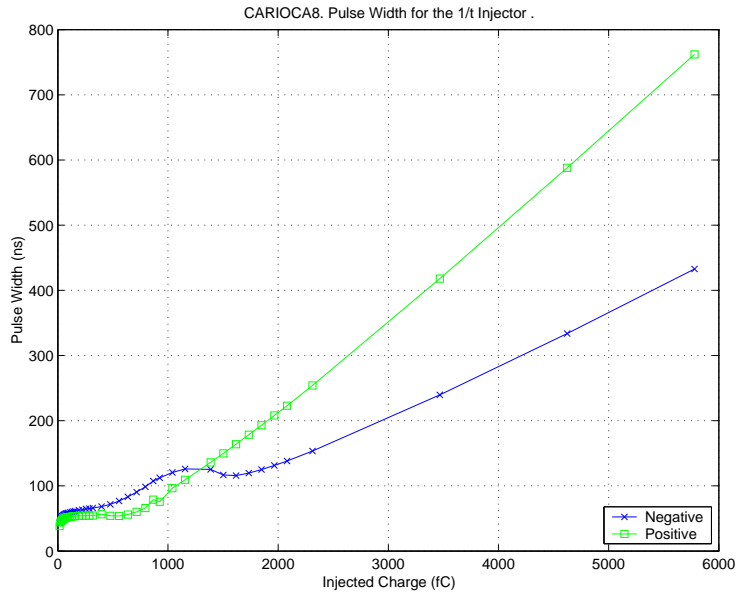
Figure 3.28: Pulse width measurements for an input charge up to 6 pC.

Changing the output resistance of the shaper or the gain of the differential amplifier would have a strong impact on the shape of the signal. This would require a tune of the time constants of the shaper and the differential amplifier. Therefore, these parameters are left untouched.

Besides reducing the time constant of the BLR two other effects are sought: increasing the maximum output current, what affects g_{m3}, and reducing slightly V_{clip} while maintaining a good matching of the transistors of the input differential pair to avoid offset problems.

Figure 3.30 shows the schematic of BLR3 for CARIOCA8. Increasing the output current was easily done by modifying the W/L of the transistors of the current mirror formed by M16, M14, M7 and M8. The original ratio between the W/L of these transistor was 4:4:4:4 while for CARIOCA8 it was changed to 1:4:4:4. This way, $I_{BLR3max}$ is three times bigger than for the previous version. This change in current produces an increase in g_{m3} which goes from 77.31 $\mu\mho$ to 170 $\mu\mho$, that is, approximately a factor 2.2.
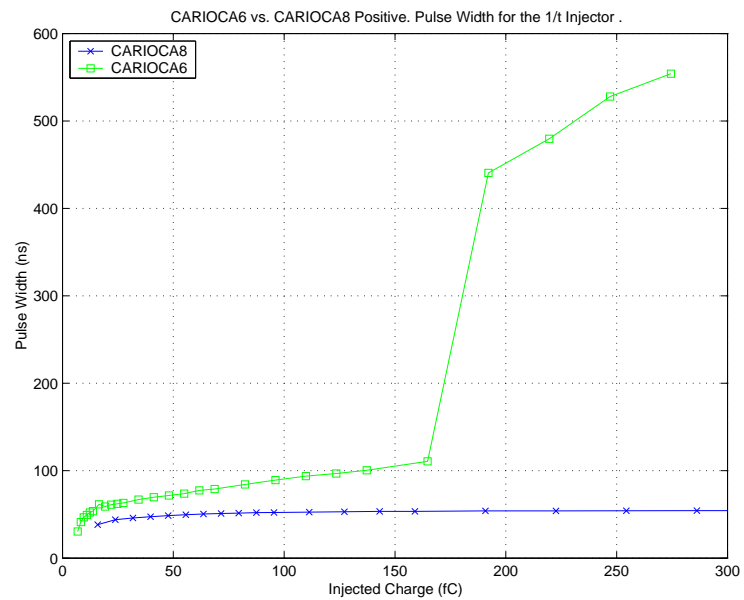
Remember also from Section 2.5 that:

$$V_{clip} = 2\frac{I_B}{g_{m1}} \tag{3.7}$$

Therefore, in order to reduce V_{clip}, g_{m1} has to be increased without changing I_B. In saturation g_m has a value of:
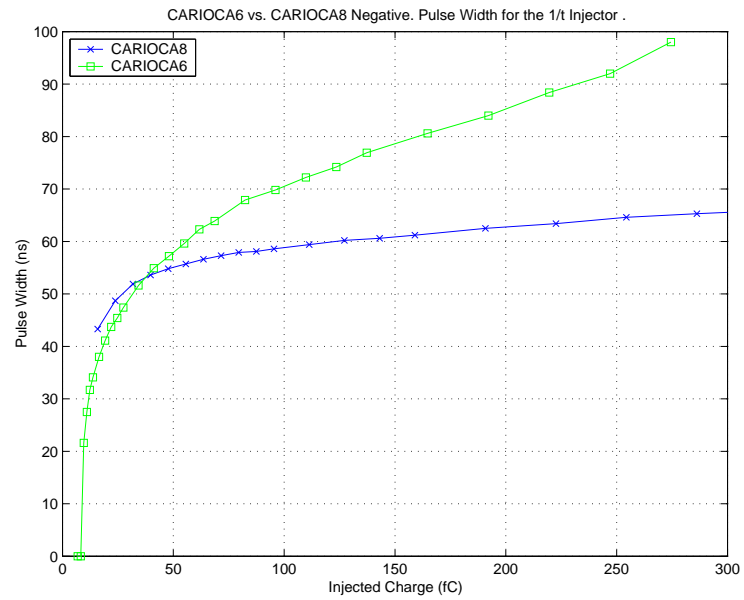
(a) Negative

(b) Positive

Figure 3.29: Comparison between the pulse width of CARIOCA6 and CARI-OCA8.
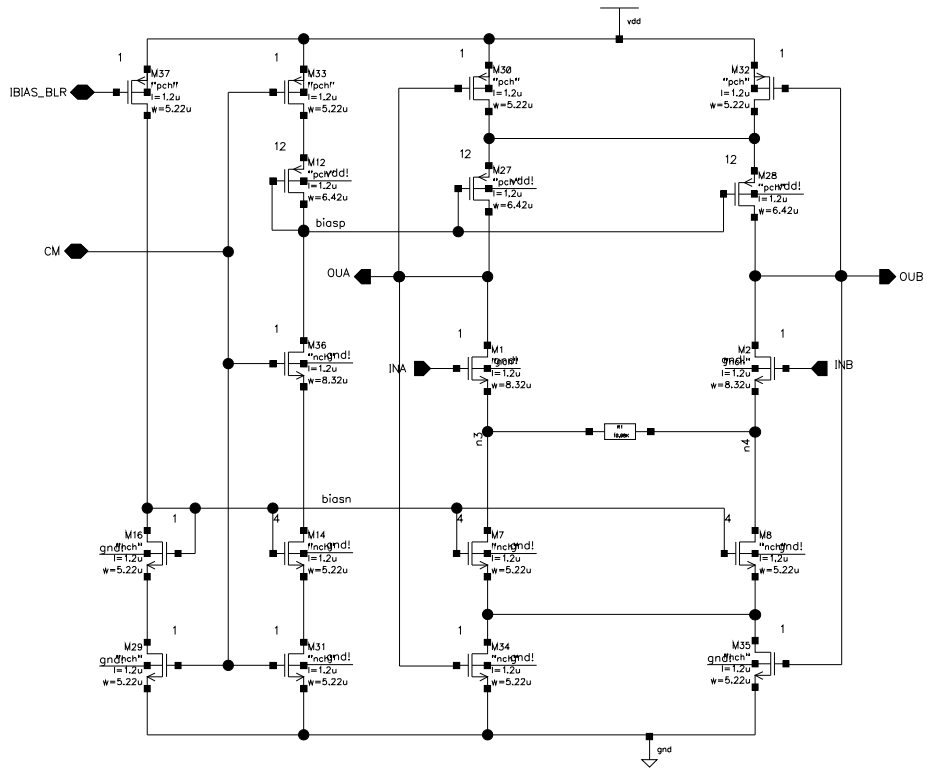
Figure 3.30: Schematic of BLR3.

$$g_m = \mu C_{ox}\frac{W}{L}V_{eff} = 2\sqrt{\frac{KP}{2n}\frac{W}{L}I_{DS}} = 2\sqrt{\frac{\beta}{2n}I_{DS}} \tag{3.8}$$

A straightforward way of changing g_m is changing W/L for the input transistors M1 and M2. This ratio changed from 4/4 to 16/4, leading to an expected factor between the original and the new g_m of approximately 4. According to simulation, the original g_m is 10.2 $\mu\mho$ and the new one 13.98 $\mu\mho$. This means that the actual factor between these two g_m is 1.37 and V_{clip} goes only from 130 mV to 107mV.

The reason for this is that for this new W/L M1 and M2 are working in weak inversion[21]. Hence, Equation 3.8 does not hold anymore, it is only valid for the strong inversion region of saturation. For the weak inversion region the value of g_m is:

$$g_m = \frac{I_{DS}}{nKT}q \tag{3.9}$$

therefore, changing W/L will not affect much g_m. The three regions in which a transistor working in saturation can be are:

$$\frac{I_{DS}}{I_{DS}^*} \gg 1 \quad \text{Strong Inversion}$$
$$\frac{I_{DS}}{I_{DS}^*} \simeq 1 \quad \text{Moderate Inversion}$$
$$\frac{I_{DS}}{I_{DS}^*} \ll 1 \quad \text{Weak Inversion}$$

where

$$I_{DS}^* = 2\beta n(\frac{KT}{q})^2 \simeq 210^{-3}\beta \tag{3.10}$$

With this new values for g_{m1} and g_{m3}, what is left is finding the appropriate value for C so that the time constant of the BLR approaches the target value of 200 ns. The chosen value is 1.728 pF. According to Equation 3.6, with C = 1.728 pF, $g_{m1} = 13.98\mu\mho$, $g_{m3} = 170\mu\mho$, $A_{diffamp} = 1.35$ and $R_{sh} = 3K\Omega$[22], the new τ would be 180 ns. Simulation gives a more accurate value of $\tau = 225ns$.

3.8   Time Walk

The time elapsed between the leading edge of the input signal and the leading edge of the output signal depends on the injected charge. This varying time walk appears because for a given threshold, the rise time of the signal in front

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[21]See [5]
[22]Values taken from simulation

of the discriminator decreases with increasing input charges. This produces different threshold crossing times.

The time walk referred to a 150 fC input signal is shown in Figure 3.31. This measurement was done together with the pulse width measurement. Therefore, channels 8 and 16 of the CARIOCA8 chips installed in board number 9 of CARIOCA7 were used. A threshold of 7 fC was used in this measurement as well. For both the positive and the negative channels the real time walk doubles the simulated time walk. Remember from Section 3.2 that the real gain up to the discriminator was 30% smaller than the simulated value. Taking this into account the factor between the real and simulated time walk is reduced to 1.5. Note that this is a very simplistic correction. The discriminator is very sensitive to the shape of its input signal. Small signals are flatter than large signals. This increases the reaction time of the discriminator. Hence, the difference between simulation and measurements is reasonable.

3.9 Radiation Tests

Cumulated irradiation effects of ionizing radiation on CARIOCA8 were tested using one of the X-Ray facilities at CERN. The average energy deposited in a material per unit of mass at the point of interest is called Dose, Absorbed Dose or Total Dose. Its units are the Gray, 1 Gy = 1 J/kg and the rad, 1 Gy = 100 rad. Remember from Section 1.4.2 that the Total Ionizing Dose (TID) CARIOCA will have to be able to absorb without misbehaving is 1MRad.

When a charged particle crosses the silicon oxide, an electron-hole pair is created. The recombination is only partial, the electrons can leave the oxide thanks to their high mobility, but most holes are trapped in the oxide due to their low mobility. This charge accumulation in the oxide produces a drift in the threshold voltage V_T.

At the Si-Si0_2 interface, interface charges are left after the crossing of a charged particle. This produces a decrease in the surface mobility. The effects on silicon are not usually permanent since the electron-hole pairs recombine they are mostly Single Event Effects (SEE).

Other total dose effects are the increase of leakage current between drain and source of the same transistor and of the leakage current between adjacent transistors[23].
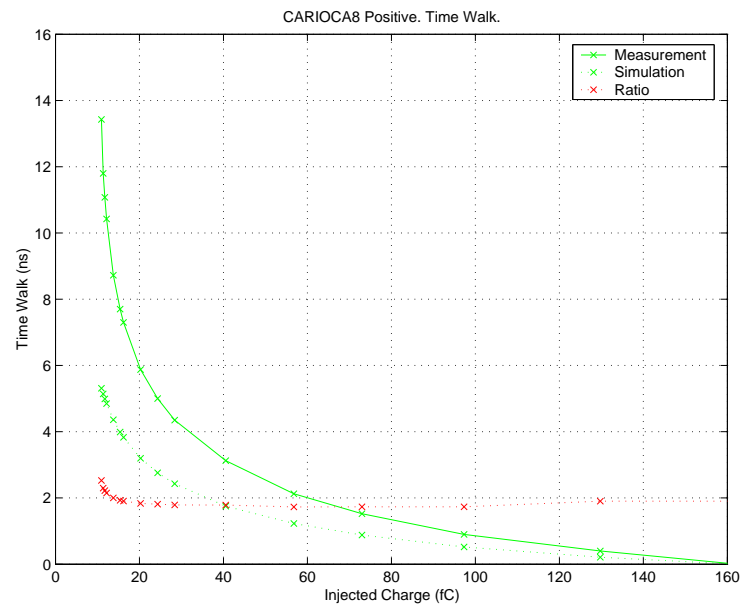
In sum, the transistor parameters that are more affected by this kind of radiation are:

- The DC current, due to the changes in the carrier mobility $\Delta\mu = \Delta\mu(TID)$ and the threshold voltage $\Delta V_T = \Delta V_T(TID)$.

- The g$_m$, also because of the changes in μ and V$_T$.

- The V$_T$ matching.

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[23]See [17]
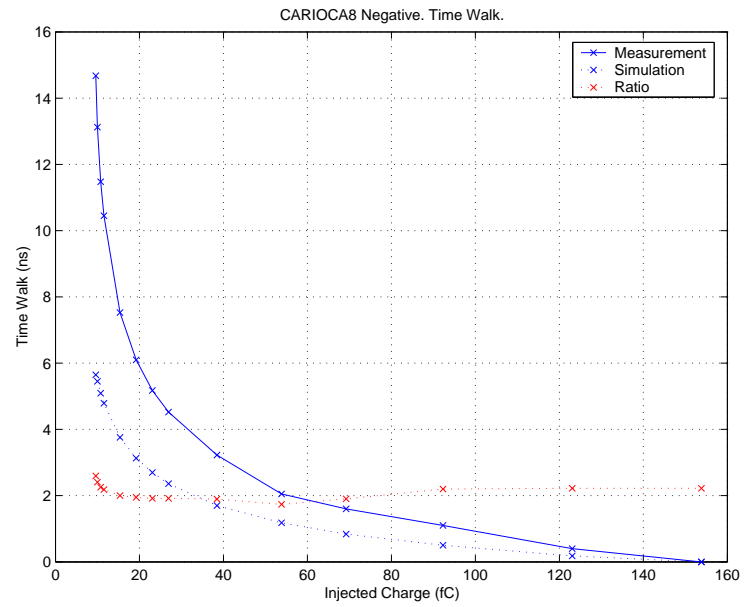
(a) Negative

(b) Positive

Figure 3.31: Time walk of CARIOCA8.

Polarity	μ Sensitivity Slope	μ Qmin Detectable
Negative	↓ 3.9%	↑ 13%
Positive	↓ 1.5%	↑ 10%

Table 3.15: Effect of the over voltage on the sensitivity.

- Noise density at the input of the transistor. It increases with the changes in g_m and the trapped charge, especially for the NMOS.

At circuit level, radiation changes the DC bias of the amplifiers, can produce instabilities, increases the noise and changes the offsets. Differential systems are more robust than their non-differential counterparts as far as radiation effects are concerned at the system level. A lot of variations in current and voltage induced by radiation are compensated by differential schemes.

Special devices with guard rings and enclosed gates are used in order to achieve a higher radiation tolerance.

The tests carried out with CARIOCA8 concern system level effects of radiation. Component level effects are not interesting as long as they do not have an impact on the function of the circuit. Both chips of board number 7 were irradiated with X-Rays. After each dose the offsets of all the channels and their sensitivity curves were measured. The average value and standard deviation of this parameters averaged for the 8 channels of these chips is shown in Figures 3.32 to 3.34. After 20Mrad, a dose 20 times higher than the expected for all the LHC life, no significant variations were detected in the sensitivity slope and the extrapolated minimum detectable charge. The offset of the threshold is the parameter that is more affected by radiation. Nevertheless, that happens for high TID and this is an effect that can be compensated by changing the threshold voltage. Even with some drifts, CARIOCA8 is fully functional for TID of up to 20 Mrad.

3.10 Over Voltage Tests

All the 16 channels of board number 7 have been working for approximately 20 hours with a supply voltage of 3.3 V when the nominal supply voltage is 2.5 V. After that time the average threshold offset of the board has been reduced by a 0.47%. The effect of this over voltage on the slope of the sensitivity and the extrapolated minimum detectable charge is shown in Table 3.15. Hence, after 20 hours of over voltage the chip is still operational even with small drifts in some of its parameters.
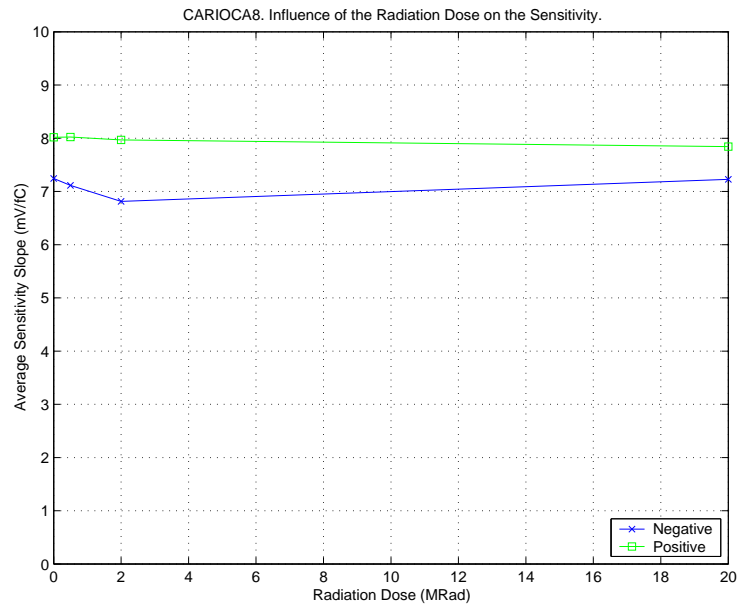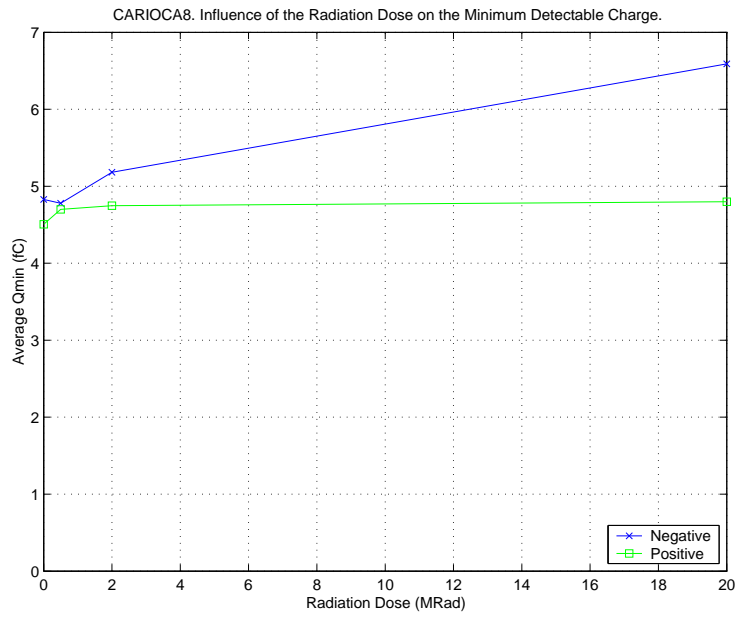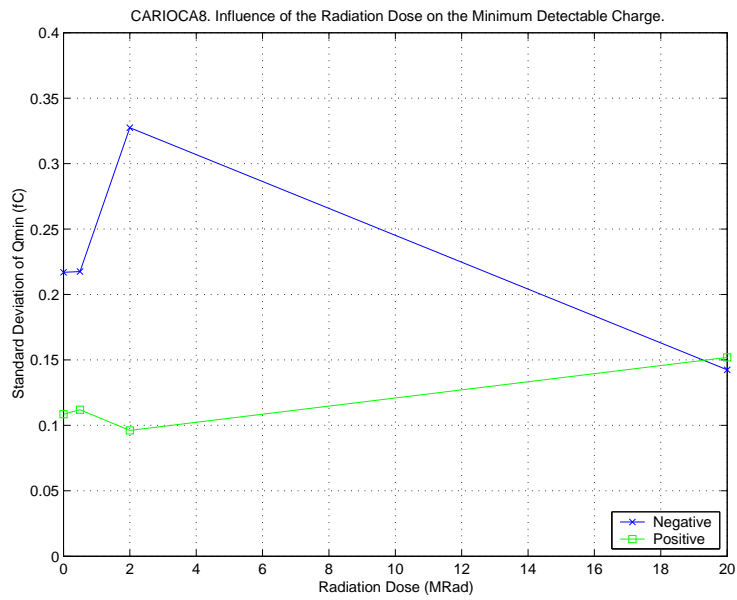
(a) Average
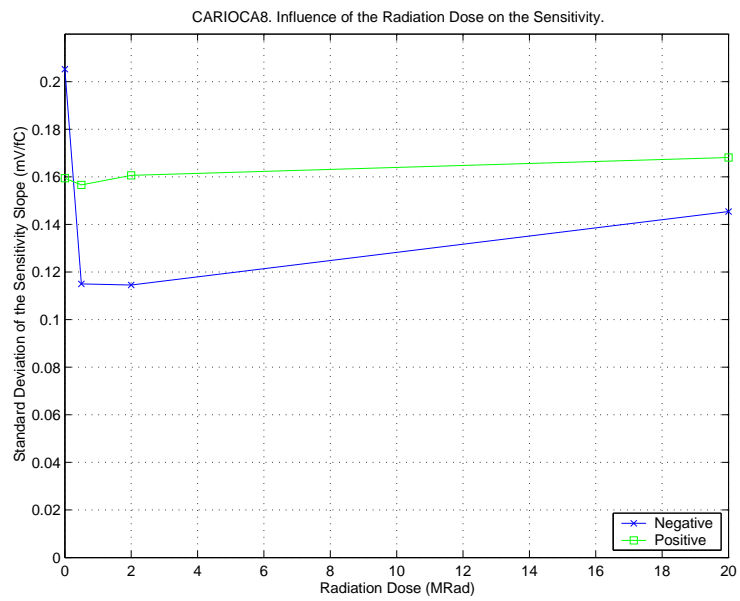
(b) Standard Deviation

Figure 3.32: Variation of the slope of the sensitivity with the Total Ionizing Dose.
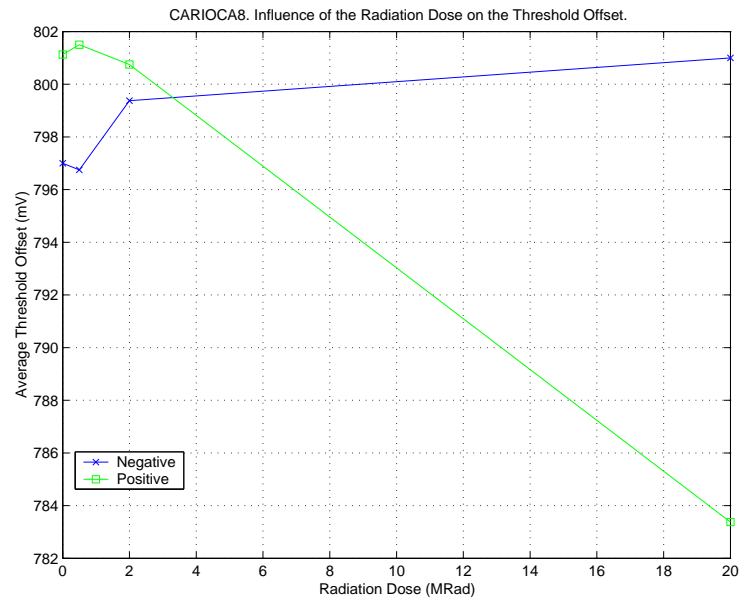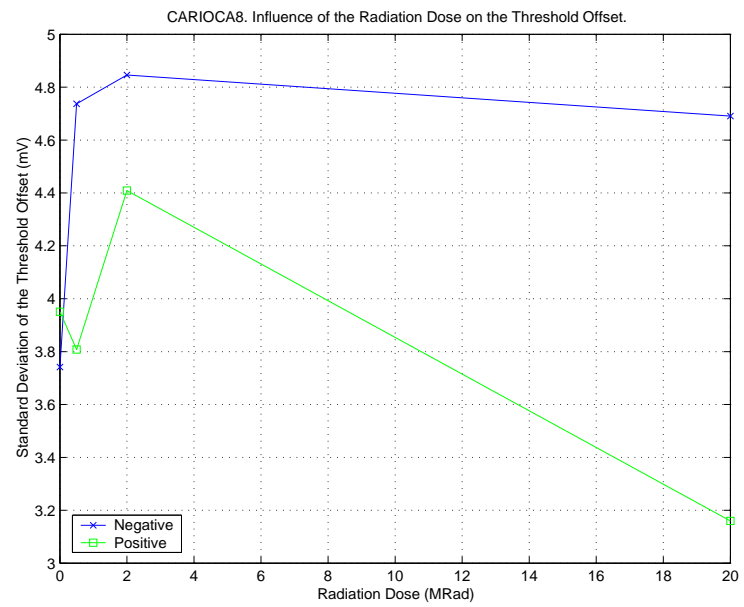
(a) Average

(b) Standard Deviation

Figure 3.33: Variation of the extrapolated minimum detectable charge with the Total Ionizing Dose.

(a) Average

(b) Standard Deviation

Figure 3.34: Variation of the threshold offset with the Total Ionizing Dose.

Parameter Name	Parameter Value
C_{det}	0 pF
I_{feed} positive	18 μA
I_{feed} negative	12 μA
I_{hyst}	6 μA
Injector	1/t
Attenuation	30dB

Table 3.16: Conditions of the temperature tests.

Parameter Name	Negative
Preamp output DC	↓ 13.75%
Vp Preamp 50 fC input	↓ 34.91%
Vp Preamp 150 fC input	↓ 29.80%
BLR- output DC	↓ 13.74%
Vp BLR- 50 fC input	↓ 26.76%
Vp BLR- 150 fC input	↓ 19.64%

Table 3.17: Percentage of variation of the preamplifier and BLR- output with temperature from 25°C to 100°C.

3.11 Temperature Tests

The behaviour of CARIOCA8 for a range of temperatures from 25°C to 100°C has been tested. The evolution with temperature of the DC level and peak voltage of the preamplifier is shown in Figure 3.35. The same results for the negative output of the BLR are shown in Figure 3.36. The measurements were done for channels 7.8 (negative) and 7.16 (positive) in the conditions of Table 3.16. Signals of 50 and 150 fC with the 1/t characteristic shape were used at the input.

The variation of the pulse width for the positive polarity channel for 50 and 150 fC is shown in Figure 3.37. The pulse width reaches its minimum for T = 60°C.

3.12 Oscillation of the Negative Preamplifier

During the measurements of the sensitivity versus detector capacitance an important discovery was done when trying to use a balanced input. The negative preamplifiers show a coherent rail-to-rail oscillation when the total capacitance connected to their inputs exceeds a certain value. CARIOCA8 counts with 16 preamplifiers, 8 for the input and 8 for the dummy input. C_{det} and C_{dummy} are connected between ground and the amplifier input. The amplifiers are sensitive to the negative polarity. Their output has negative polarity and produces a perturbation of this polarity in the ground to which all the preamplifiers and input capacitors are connected. This perturbation is sensed by the capacitors
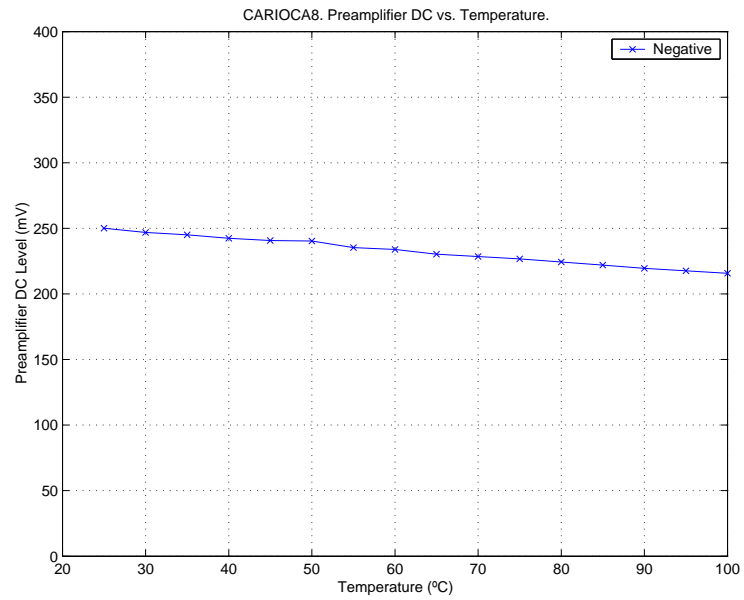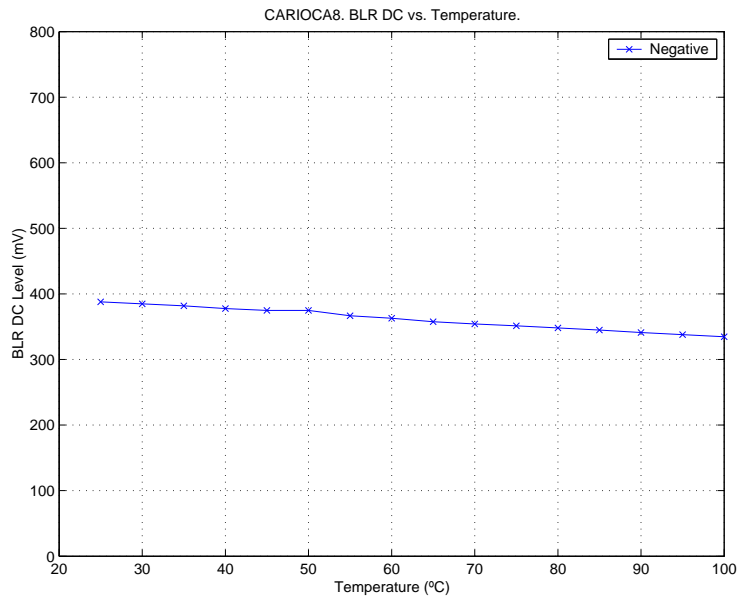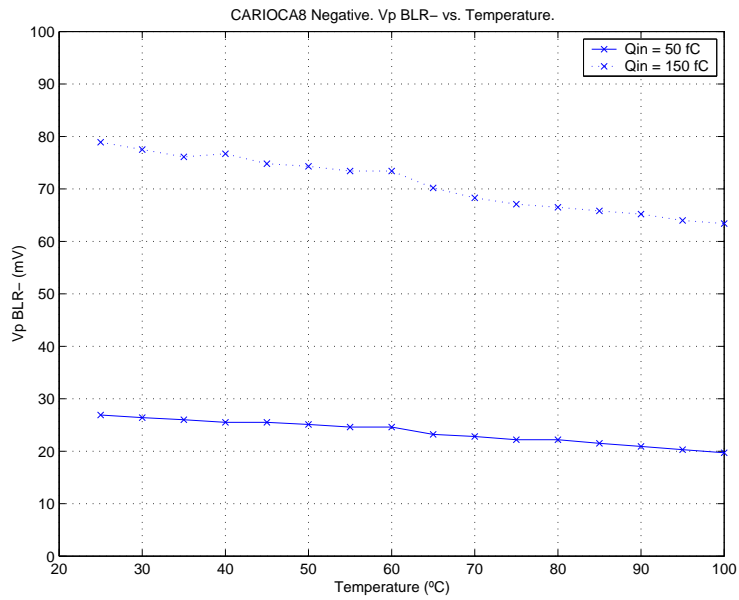
(a) DC Level
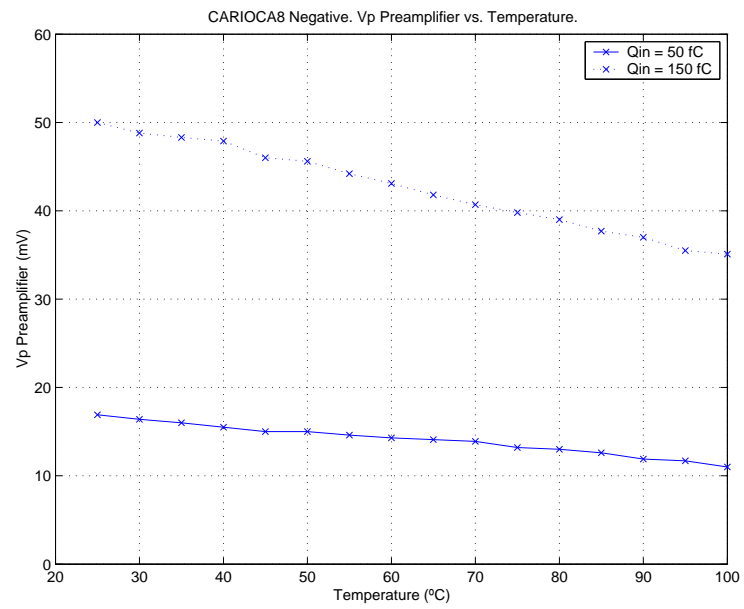
(b) Peak Voltage

Figure 3.35: Variation with temperature of the measured DC level and peak voltage of the negative preamplifier for a 1/t input of 50 and 150 fC.

(a) DC Level

(b) Peak Voltage

Figure 3.36: Variation with temperature of the measured DC level and peak voltage of the BLR for a negative channel for a 1/t input of 50 and 150 fC.
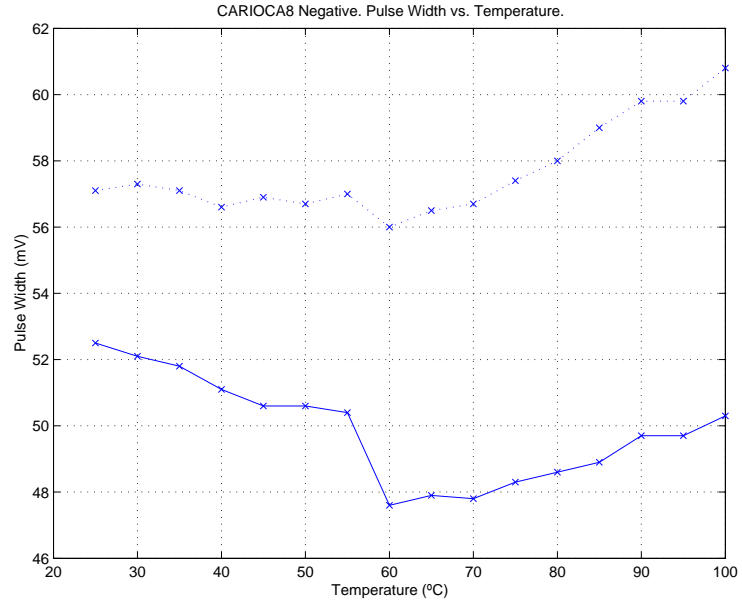
Figure 3.37: Variation with temperature of the pulse width for a negative channel for a 1/t input of 50 and 150 fC.

and, when they have a large enough value, this perturbation is amplified over and over again by the amplifiers. This is the way this oscillation is built up, because of a positive feedback loop through the ground trace of the negative preamplifiers. Expressed mathematically, when an initial charge Q_0 is injected in one preamplifier, after going through the amplifier and being feed backed through the ground trace, it produces a charge $Q_1 = kQ_0$ that is sensed by the 16 preamplifiers. Thus, after this charge has gone through the amplifiers and the feedback loop, the charge that can be found at the input of the 16 amplifiers is $Q_2 = 16kQ_1 = 16kkQ_0$. n iterations of this process produce an input charge of

$$Q_n = (16k)^n kQ_0 \tag{3.11}$$

This system will oscillate when

$$16^n k^{n+1} \geq 1 \tag{3.12}$$

that is, when

$$k \geq \frac{1}{16} \tag{3.13}$$

k is a coefficient that includes the gain of the amplifier and of the feedback loop. It expresses the relation between the charge at the input of the amplifier and the charge that is feed backed from the output to the input of the amplifier.

This problem is not present in a chip configured to be sensitive to the positive polarity since the output of the preamplifier is also negative for this case, therefore there is not a positive feedback loop in this case and the current pulled from the ground line of the power supply has a peak value 6 times smaller (0.16 mA for the positive versus 1 mA for the negative in simulation).

This oscillation of the negative preamplifiers is not sensed further in the circuit. The differential input differential output shaper is so well matched that there is no output signal after it even having all the 16 preamplifiers oscillating coherently rail-to-rail. The rest of the circuit is silent while the preamplifiers are constantly consuming power and preventing the chip from working properly.

This effect had not been seen in simulation before because all the circuits were connected to ideal ground. Introducing an impedance between the ground of the board, to which the capacitors are connected, and the preamplifiers ground reveals this effect also in simulation, even considering only two amplifiers. An estimation of the actual resistance and inductance of the ground traces is very difficult to do. Moreover, their value will increase with the package of the chip. Therefore, some typical values were used in the simulations. Simulation results are shown in Figures 3.38 and 3.39.
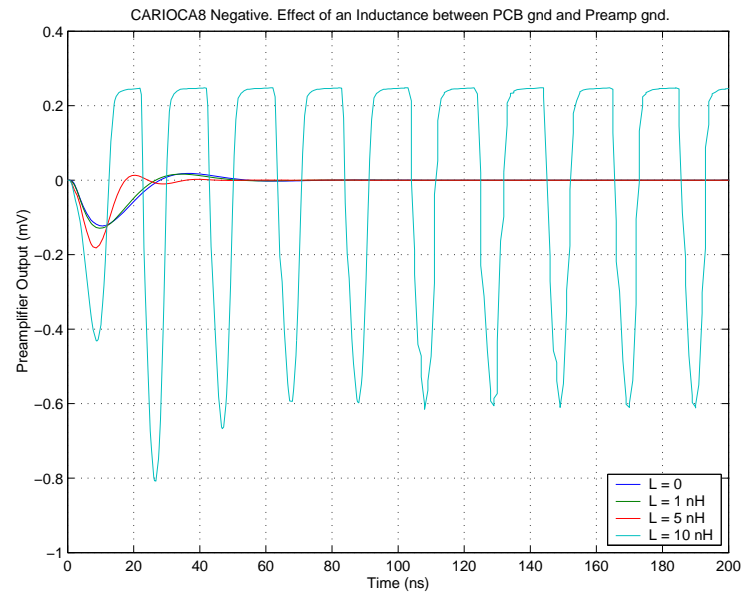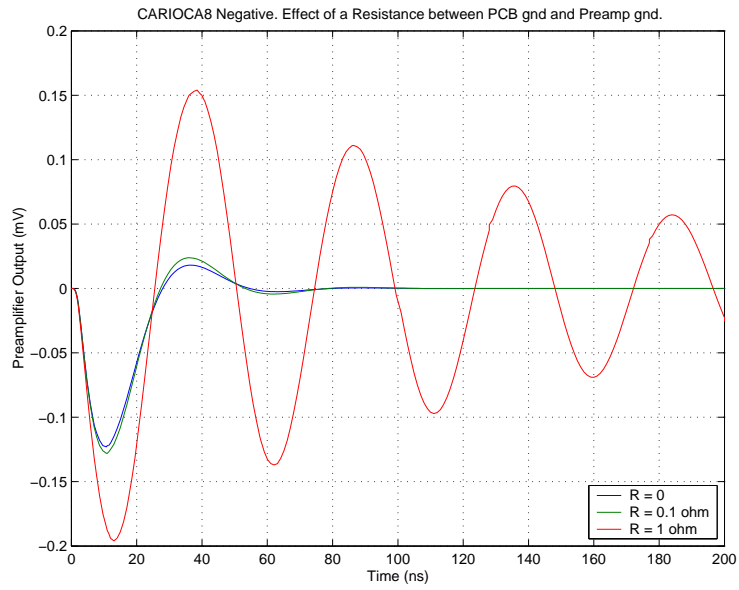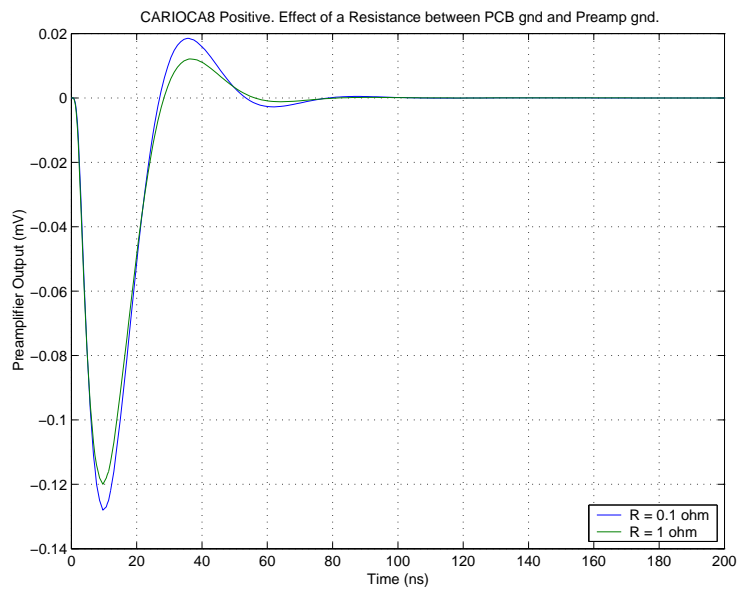
(a) Negative
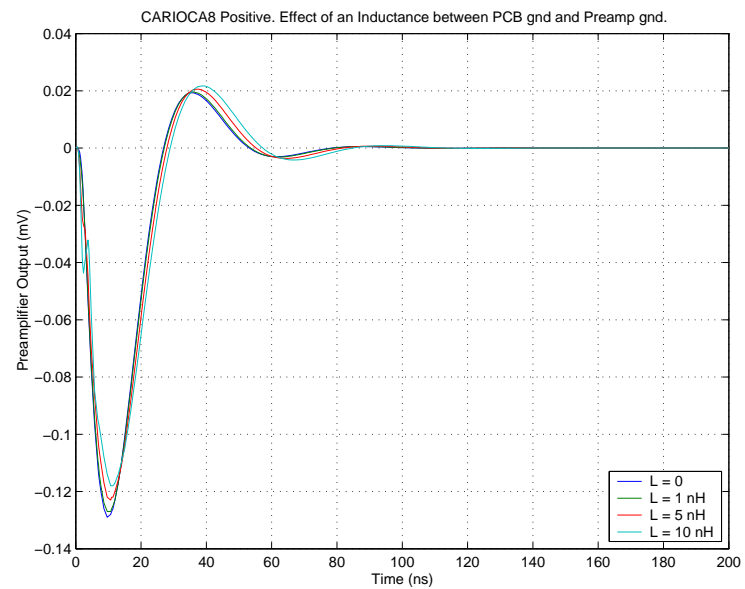
(b) Positive

Figure 3.38: Effect of an inductance between the ground trace of the PCB and the ground of the preamplifier.

(a) Negative

(b) Positive

Figure 3.39: Effect of a resistance between the ground trace of the PCB and the ground of the preamplifier.

Chapter 4

Conclusions and Future Work

During the realization of this thesis several problems of various CARIOCA prototypes have been identified. The test of CARIOCA8 has shown that the changes introduced in CARIOCA6 and CARIOCA7 in order to solve them have been succesful. A test system has been implemented in order to automatize time consuming measurements such as sensitivity and offset measurements. This has made feasible the realization of tests that involve multi channel statistics.

CARIOCA8 has been fully characterized and already meets nearly all the specifications set for the readout electronics of the muon system of LHCb. The required linear range is widely exceeded, the offsets are inside the permitted range, the influence of process variations in the sensitivity produces only small drifts between the sensitity of different channels, increasing detector capacitances worsen the noise figure as expected, the chip is radiation hard and resists high temperatures and over voltage at the power supply lines without significant variations in its performance.

Two problems discovered while testing CARIOCA8 prevent the chip from meeting specifications. The first one is related to the pulse width of the output signal, which is slightly larger than the target value of 50 ns for charges up to 150 fC. In order to solve this, CARIOCA10 will modify slightly the shaping of the signal and implement a more agressive baseline restoration.

The second problem is related to the behaviour of the negative preamplifier. There is a significant difference between the simulated and the real shape of the signals leaving the negative amplifier. The simulations and tests done on CARIOCA8 showed as well that for large number of amplifiers (16) and large detector capacitances the coupling of the output signal to the input through the ground trace can lead the amplifiers into oscillation. CARIOCA9 has an improved ground distribution that will reduce the ground impedance and, therefore, the probability of having oscillations. Nevertheless, packaging the chips will increase this impedance again. Hence, other measures have been taken. CAR-

IOCA10 will improve the design of the negative amplifier. It is expected that these changes will make disappear the disagreement between simulated and real shape and the risk of oscillation. This prototype will be submitted by the end of June, 2003 and will be tested approximately three months later.

Some CARIOCA8 chips have been sent for packaging. This will allow to test the impact of a QFP[1] in the performance of the ASIC.

Apart from the two problems mentioned above, the chip meets all the other specifications and if the changes introduced in the design work as expected, it will be ready for production in time for the LHCb project.

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[1] Quad Flat Pack

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