CARIOCA 10th prototype
June 2003 submission

ARCHITECTURE & LAYOUT OVERVIEW

Nicolas PELLOUX

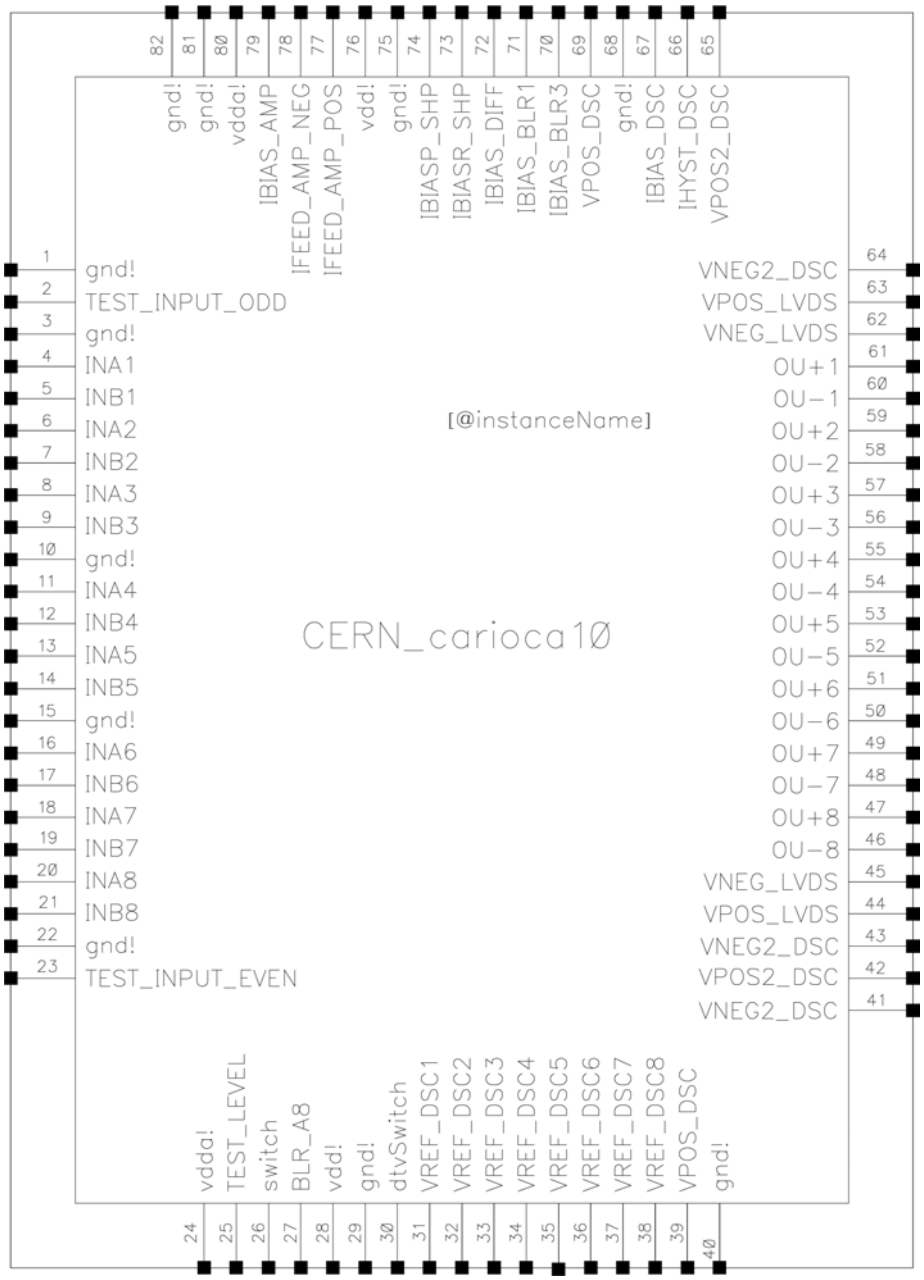

TABLE OF CONTENTS

1 New Preamplifier 5
1.1 Transistor bias improvement 5
1.2 Changes on the feedback architecture 5
1.3 Phase margin improvement 7
1.4 Input impedance improvement 9
1.5 Sensitivity to temperature, power supply and process 10
1.6 Preamplifier linearity 10
1.7 Channel sensitivity 11
2 Chip framework 13
2.1 The “switch” control signal 13
2.2 Internal test structure 13
2.3 Bias network 15
2.4 DTV’s 15
2.5 Internal pads 18
3 Ground and power supply lines distribution 19
4 ESD protections 20
5 Chip pads 21
5.1 Pads description 21
5.2 Pads for the bias 24
6 Chip floorplanning and layout 25
7 Libraries and files 29
7.1 The Libraries 29
7.2 Libraries architecture 29
7.3 Where to find the library files 29
7.4 Where to find the submission files 30
8 LVS matching 31

TABLE OF FIGURES

Figure 1. New bipolar preamplifier schematic 6
Figure 2. Negative polarity preamplifier simplified schematic 7
Figure 3. Positive polarity preamplifier simplified schematic 7
Figure 4. Negative preamplifier output 8
Figure 5. Positive preamplifier output 9
Figure 6. Input Impedance for the negative polarity preamplifier 10
Figure 7. Preamplifier linearity for Cdet = 0pF 11
Figure 8. Channel sensitivity for Cdet = 10pF 12
Figure 9. Channel sensitivity for Cdet = 220pF 12
Figure 10. Channel block diagram 13
Figure 11. Internal test structure 14
Figure 12. Differential Threshold Voltage (DTV) 15
Figure 13. DTV features 16
Figure 14. DTV simplified schematic 16
Figure 15. The control signal “dtvSwitch” 17
Figure 16. Internal pads and analog buffer 18
Figure 17. Ground and power supply lines distribution 19
Figure 18. ESD strategy 20
Figure 19. Chip pads 23
Figure 20. Layout : the 8 channels and the 8 DTV's 25
Figure 21. Layout : one channel, DTV, bias network 26
Figure 22. Layout : channel description 26
Figure 23. Layout : internals pads and internal test structure 27
Figure 24. Layout : 6 diode chain cells 27
Figure 25. Layout : 2 power clamp cells 28

TABLE OF TABLES

Table 1. Sensitivity to temperature, power supply and process..... 10
Table 2. Pads description..... 21
Table 3. Pads for the bias..... 24
Table 4. CARIOCA libraries..... 29
Table 5. Standard libraries used..... 29
Table 6. Carioca library paths..... 29

1 New Preamplifier

1.1 Transistor bias improvement

Few transistors did not have a correct bias in the preamplifier cell. For example some cascode transistors had their Vds smaller than their Vdssat. Some of them had then been removed. And also, all the other transistors bias have been checked and corrected if necessary.

- At room temperature,
- For high temperature (125 °C),
- For power supply variation +/- 10 % and
- For process variation +/- 3 sigma.

1.2 Changes on the feedback architecture

In fact, the negative channel was not really stable, especially when introducing both a few ohms in between the substrate and the board ground and the detector capacitance. This was actually coming from a branch in the feedback for which the DC current was signal dependent.

In the previous preamplifier schematic, there was the input stage (M36 and M35 in Figure 1) which is common for the two polarities, and the first stage of the feedback (Yellow transistor M91 in Figure 1) which was also common for the 2 polarities, and then there were 2 independent circuitries for positive and negative polarities.

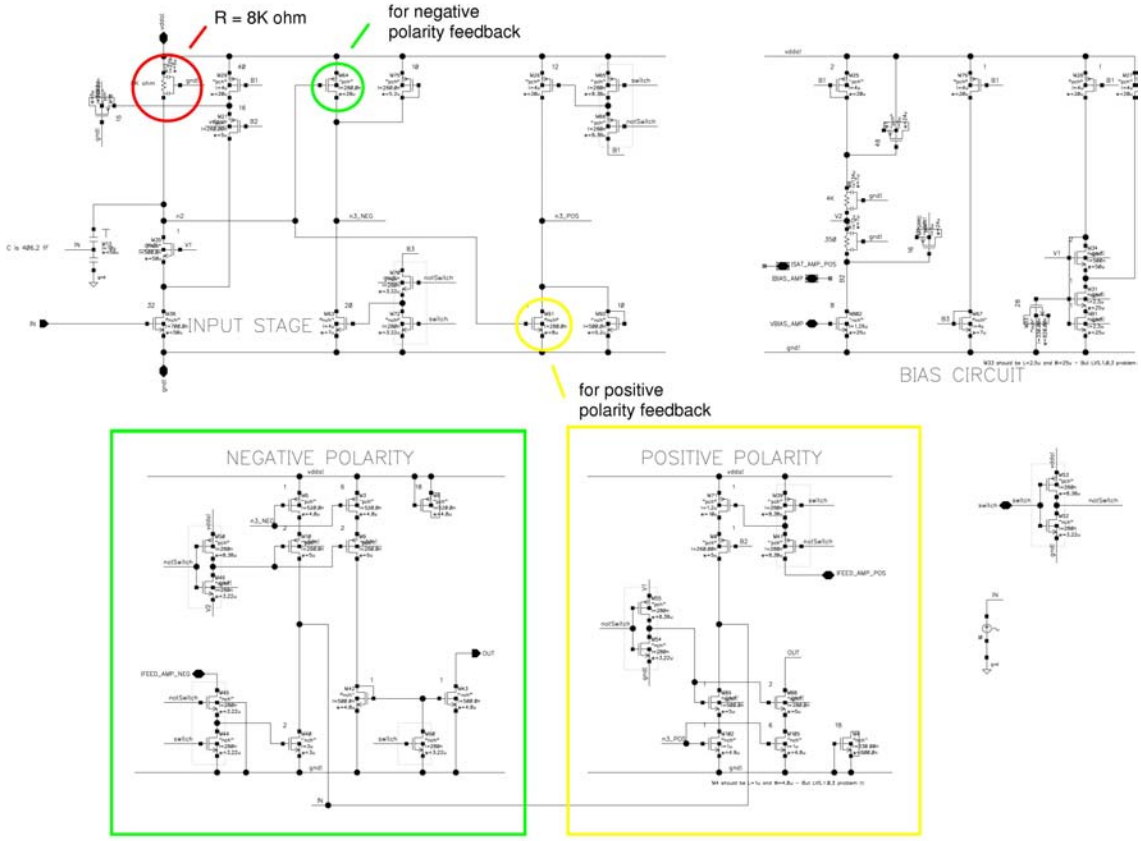

Figure 1. New bipolar preamplifier schematic

Now the separation in between the positive and negative polarity feedback circuit starts earlier in the preamplifier schematic. The feedback circuit for the positive polarity is unchanged and starts at the transistor M91 in yellow (Figure 1). The feedback circuit for the negative polarity starts at the transistor M64 (Figure 1) in green.

From simulation, the negative channel is not anymore sensitive to a resistance in between substrate and board ground. And it behaves like the positive one.

The two following figures show the simplified schematics of both the negative and positive polarities preamplifiers.

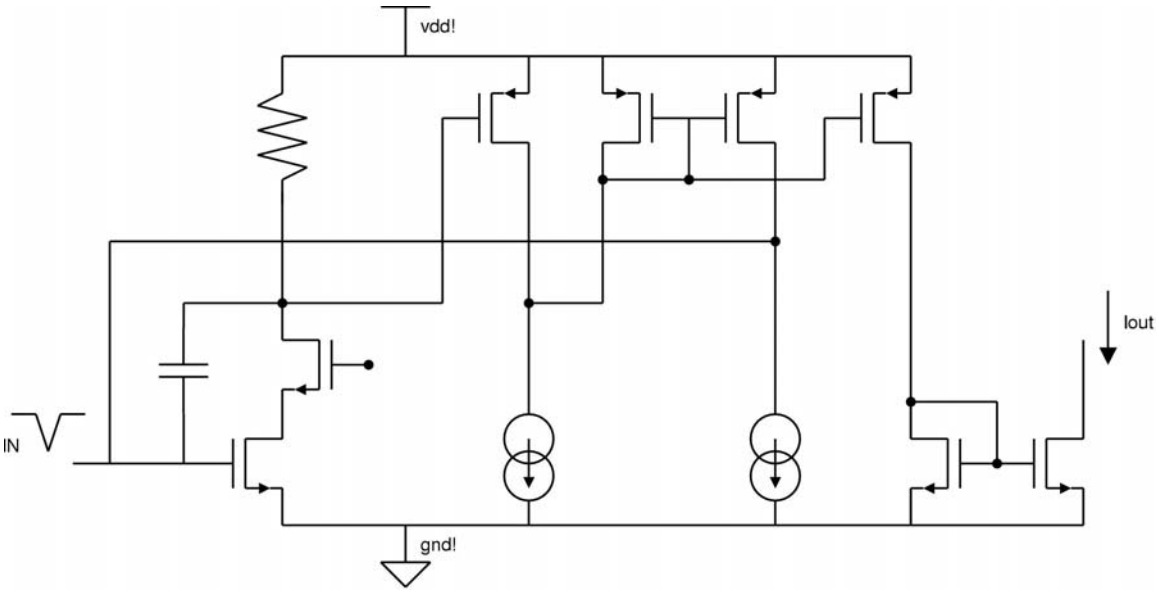

Figure 2. Negative polarity preamplifier simplified schematic

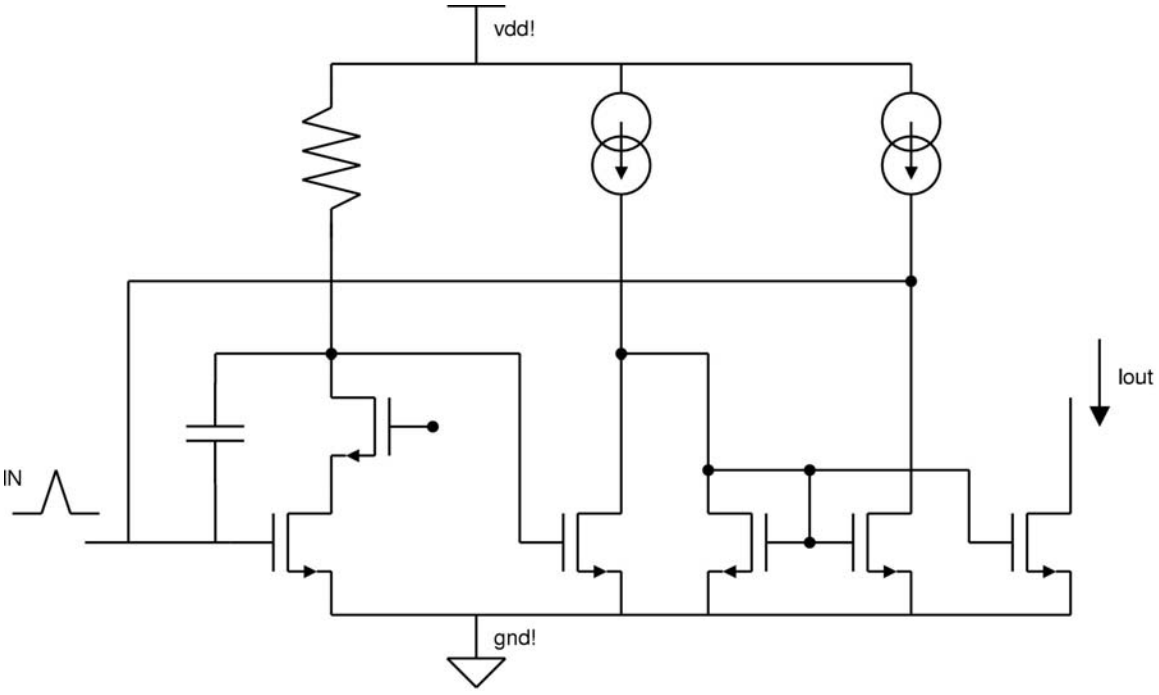

Figure 3. Positive polarity preamplifier simplified schematic

1.3 Phase margin improvement

At the input stage, we replaced the current source transistor by an 8 Kohm resistor in red (Figure 1, Figure 2 and Figure 3). This reduces the voltage gain of the input stage,

increases the phase margin and the input impedance as well, and thus reducing the sort of inductive behavior at the input.

Now the phase margin for the negative preamplifier are respectively 79.8 deg and 76 deg for 0 pF and 220 pF detector capacitance.

And the phase margin for the positive preamplifier are respectively 76 deg and 67 deg for 0 pF and 220 pF detector capacitance.

The following figures (Figure 4 and Figure 5) show the transient output of the preamplifier for different detector capacitances.

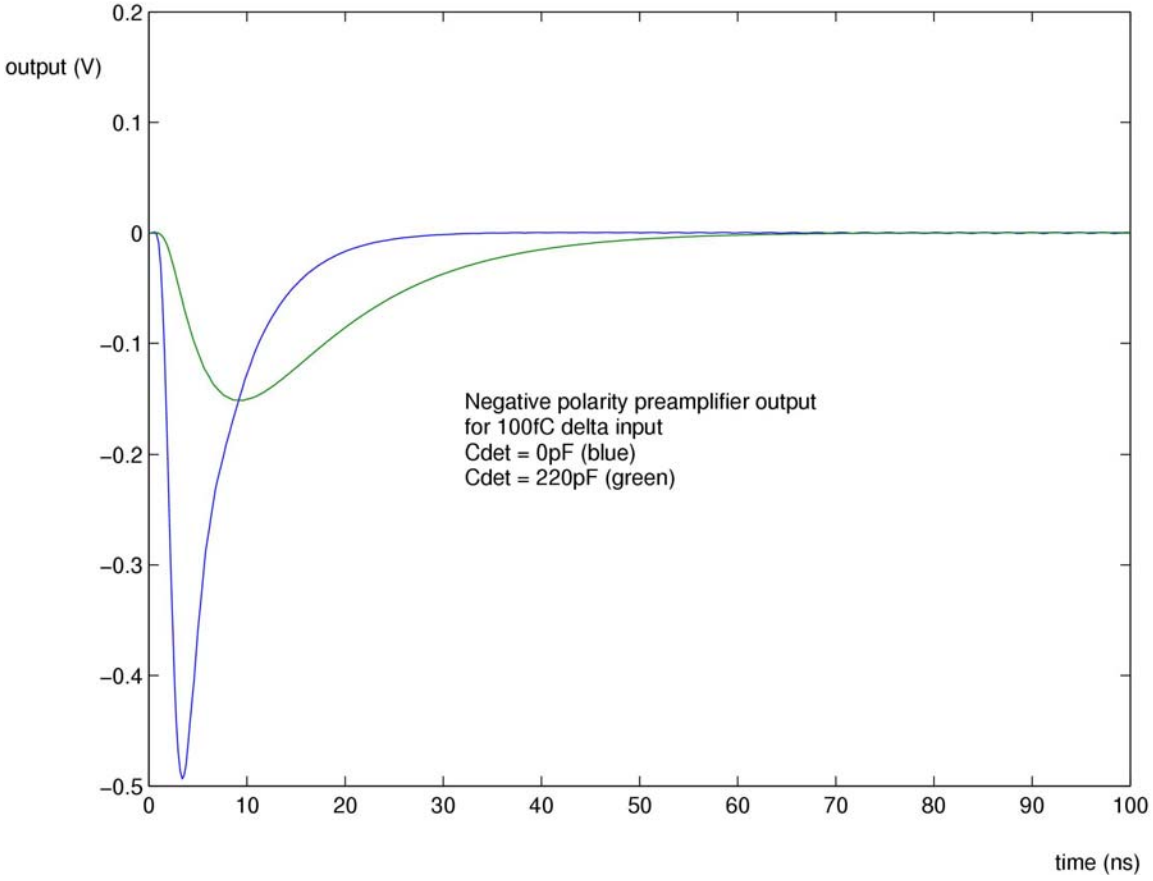

Figure 4. Negative preamplifier output

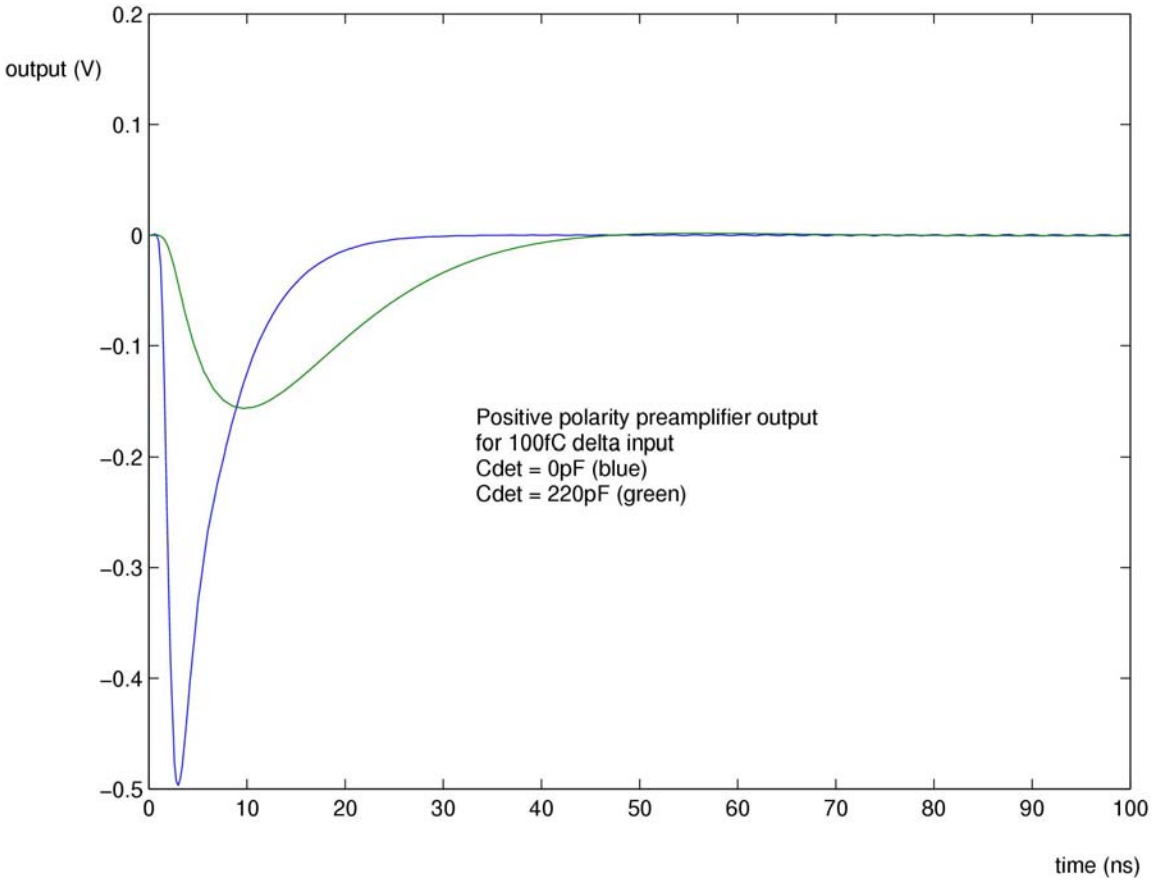

Figure 5. Positive preamplifier output

1.4 Input impedance improvement

The input impedance is now around 45 ohm instead of 5 ohm for the previous version. There is still a small inductive effect for 0pF detector capacitance. This effect is attenuated as soon as a detector capacitance of few ohms is present.

The Figure 6 shows the preamplifier input impedance for 220pF and 0pF detector capacitance. The input impedance for the positive polarity preamplifier is not as shown as it is really close to the negative one.

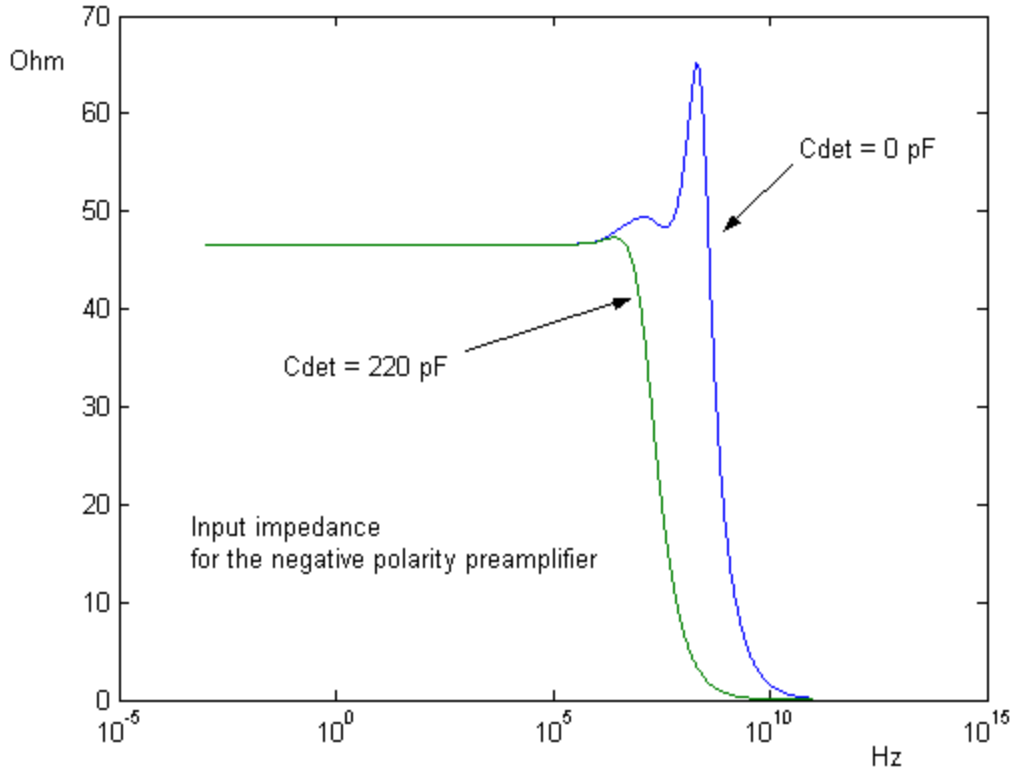

Figure 6. Input Impedance for the negative polarity preamplifier

1.5 Sensitivity to temperature, power supply and process

The following Table 1 gives the sensitivity of the preamplifier output signal amplitude for parameters variations.

Table 1. Sensitivity to temperature, power supply and process

	Negative polarity preamplifier	Positive polarity preamplifier
Temperature (125 °C)	14 %	24 %
power supply variation +/- 10 %	9 %	7 %
process variation +/- 3 sigma	12 %	14 %

1.6 Preamplifier linearity

The two following charts (Figure 7) show the linearity of the preamplifier for the negative and the positive polarities. The bipolar preamplifier is linear up to 200fC input charge for both polarities.

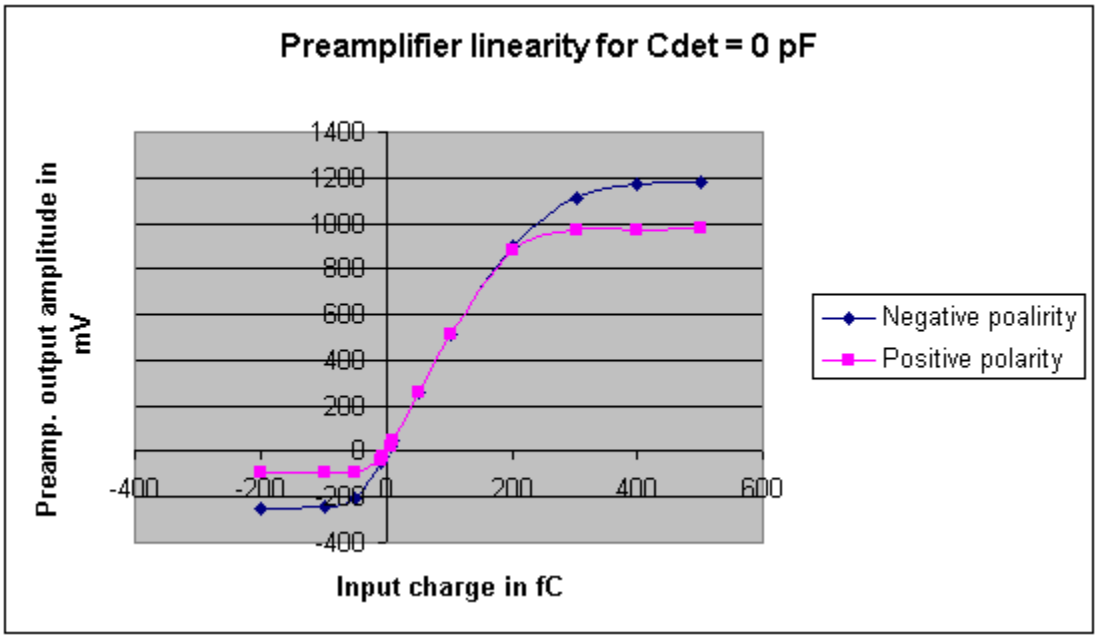

Figure 7. Preamplifier linearity for Cdet = 0pF

1.7 Channel sensitivity

The two following charts (Figure 8 and Figure 9) show the sensitivity of the channel. Vthreshold (outside) corresponds to the voltage VREFA-VREFB (Figure 12) applied to the discriminator and the amplitude (inside) corresponds to the amplitude pick to pick of the signal at the discriminator input.

At 10pF detector capacitance, the maximum input charge is 17fC. Over 17fC input charge, the discriminator always discriminates even with a large Vthreshold (outside) of 2.5V. The sensitivity is 23mV/fC referring to Vthreshold (outside) and to VREF_DSC as well (Figure 13 and Figure 14).

Similarly, at 220pF detector capacitance, the maximum input charge is 31fC and the sensitivity is 12mV/fC referring to Vthreshold (outside) and to VREF_DSC as well (Figure 13 and Figure 14).

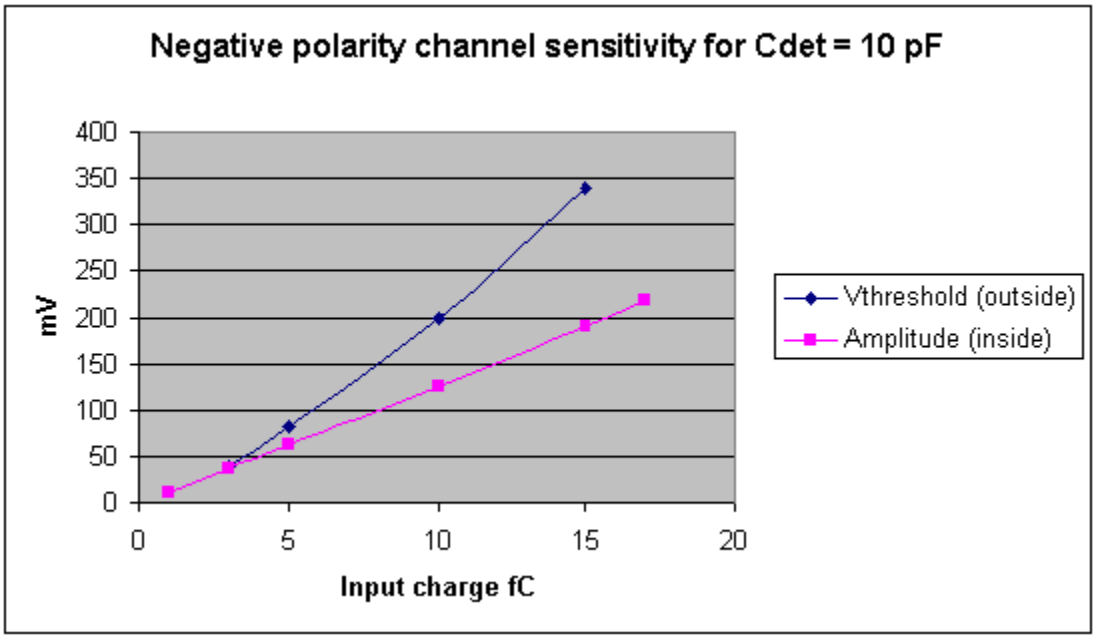

Figure 8. Channel sensitivity for Cdet = 10pF

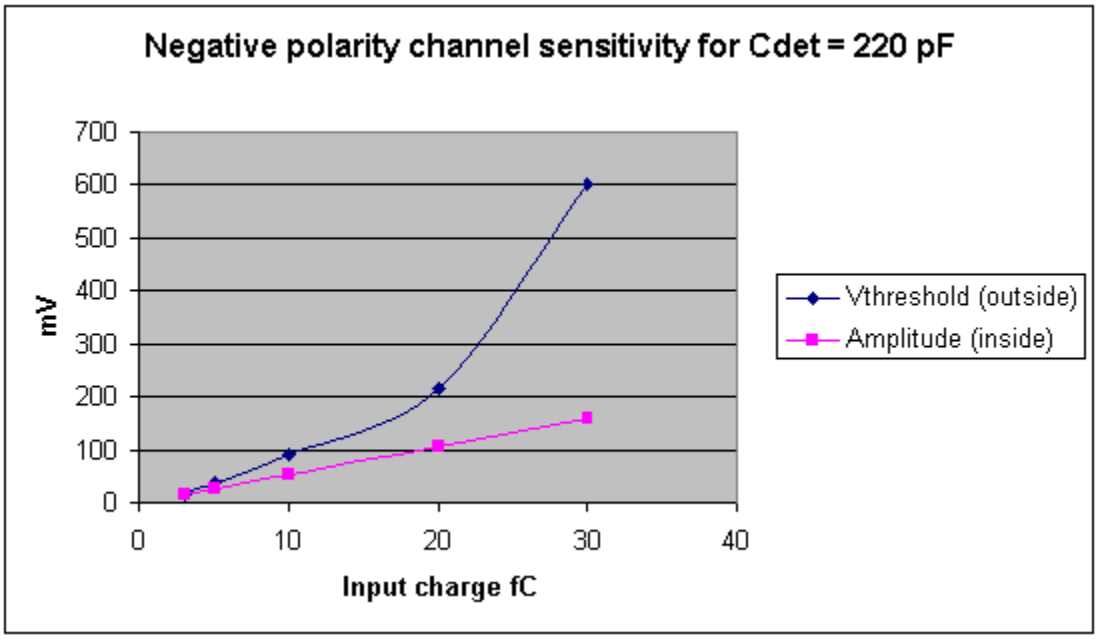

Figure 9. Channel sensitivity for Cdet = 220pF

2 Chip framework

Carioca chip prototype from June 2003 submission, has 8 channels. One channel consists in (Figure 10) :

- Two preamplifiers, the one that receives the signal and the dummy one,
- The shaper with 2 poles and 2 zeroes for tail cancellation,
- The differential amplifier with one pole and one zero for shaping
- The Base Line Restoration (BLR) circuit to keep the signal average near the common-mode voltage
- The discriminator
- The LVDS with two differential outputs.

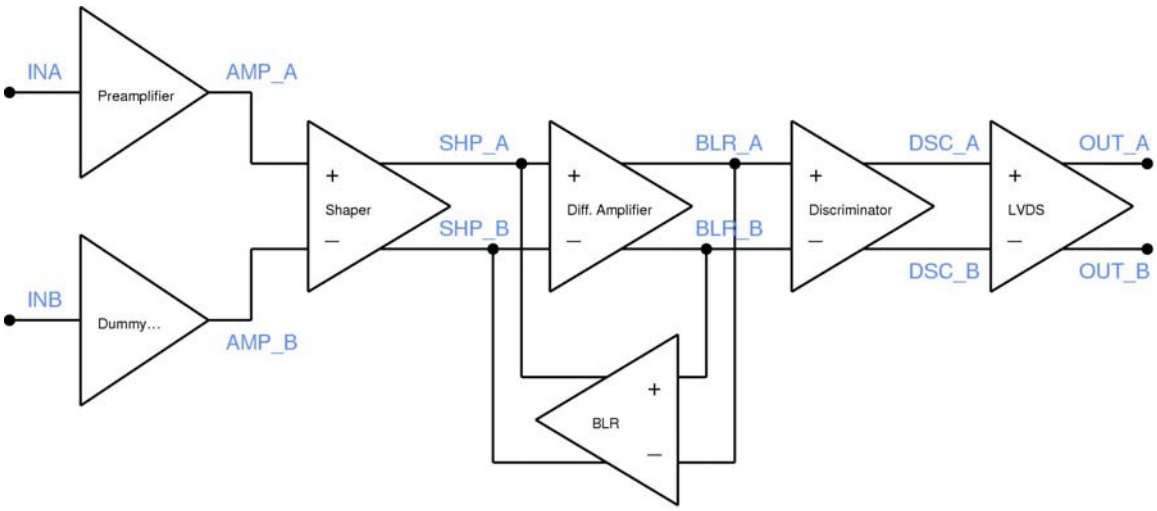

Figure 10. Channel block diagram

2.1 The "switch" control signal

One preamplifier itself consists actually in 2 preamplifiers : one for positive polarity signals and one for negative polarity signals. A control signal allows to select one of them, keeping the other one quiet by switching its DC current sources off. When the control signal is set to 0 volt, the negative polarity preamplifier is selected. When the control signal is set to 2.5 volt, the positive polarity preamplifier is selected.

2.2 Internal test structure

On chip, an internal test structure allows us to inject a charge from 50fC to 125fC to the channels input. A serial input charge capacitance of 50fF is connected to the preamplifier (Figure 11).

This 50fF capacitance is made using the parasitic capacitance in between two metal planes M1 and M2 in order to minimize the area.

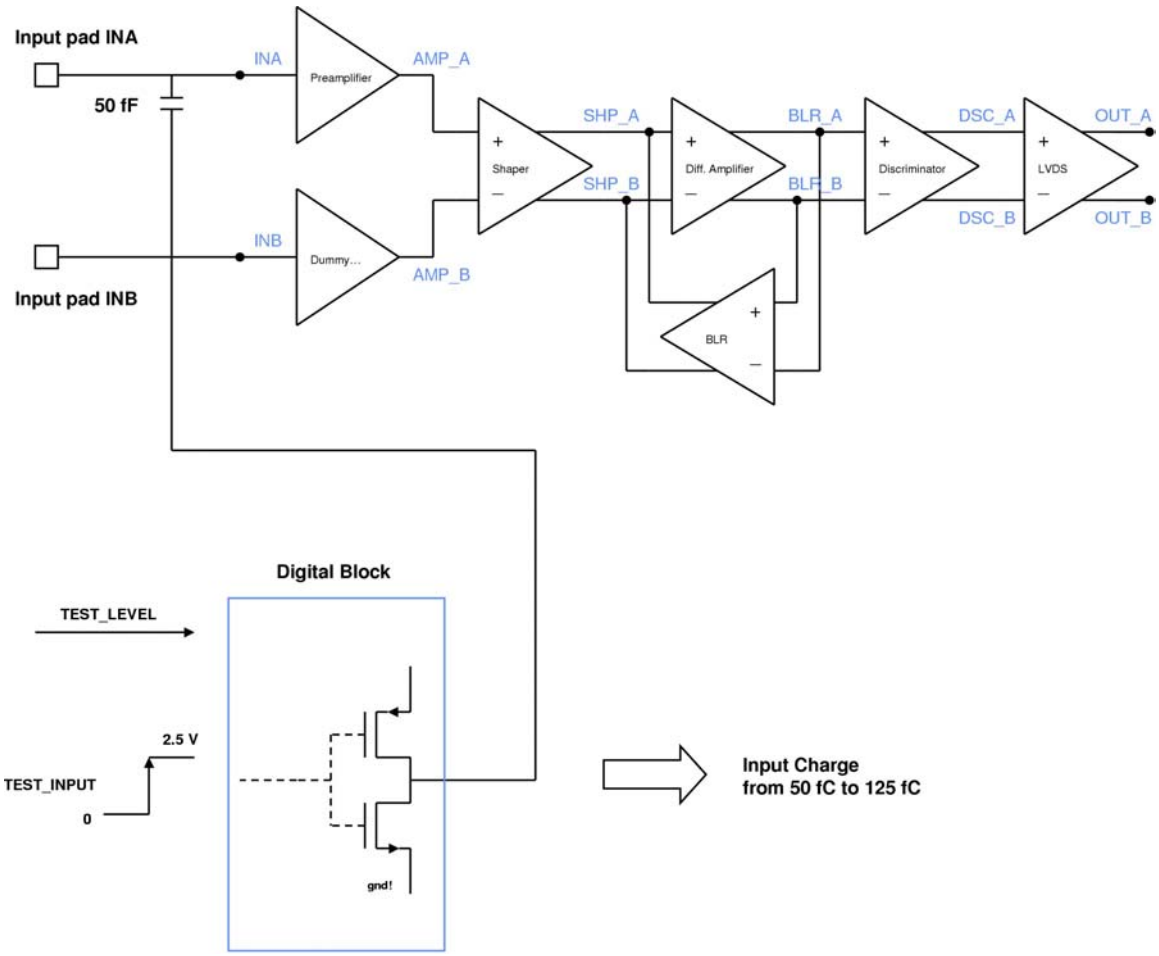

Figure 11. Internal test structure

The TEST_LEVEL voltage controls the value of the input charge. For TEST_LEVEL equal to 2.5 volt, the input charge is maximum : 125 fC. For TEST_LEVEL equal to 1 volt, the input charge is minimum : 50 fC. If the TEST_LEVEL control is less than 1 volt, the digital block does not work properly.

The TEST_INPUT has always to be a fast signal rising from 0 to 2.5 volt. This TEST_INPUT signal fires the digital block, and then injects the charge into the preamplifier. This digital bock consists of 3 NAND gates. It allows us to have a negative polarity or a positive polarity input signal depending on the preamplifier polarity we are using, which means depending on the binary value of the control signal “switch”.

Actually on chip, there are two TEST_INPUT signals :

- The TEST_INPUT_ODD signal that fires all the odd channels, and
- The TEST_INPUT_EVEN signal that fires all the even channels.

2.3 Bias network

For all the different blocks in the channel, except for the LVDS, there is a bias network. This bias network splits the current mirrors and connects then the gates of the current source transistor of the 8 channels.

2.4 DTV's

DTV means Differential Threshold Voltage. For each discriminator (8 in total), a threshold as to be set. The signal is fully differential at the input of the discriminator. The threshold voltage has to be set in a differential way as well : VREFA and VREFB (Figure 12).

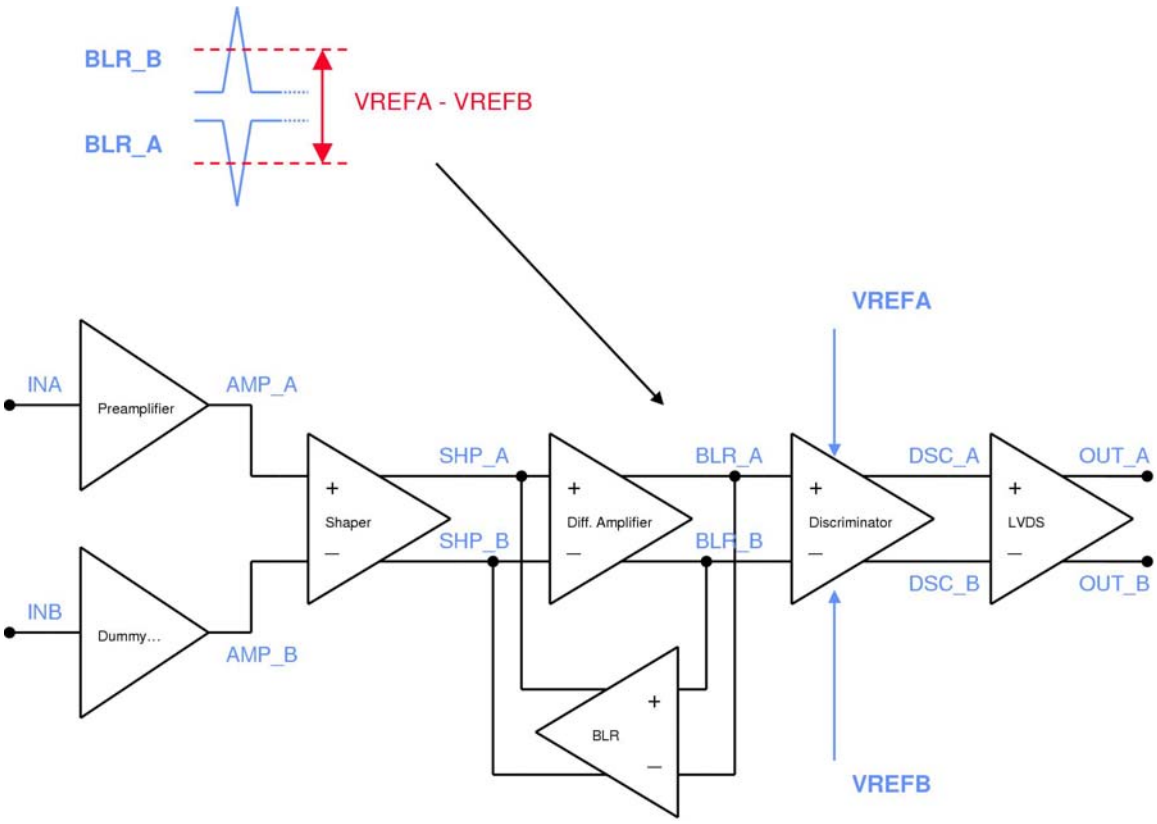

Figure 12. Differential Threshold Voltage (DTV)

Given a reference voltage VREF_DSC varying from 0.8 to 2.0 volts, the role of the DTV is to give a differential signal VREFA and VREFB with (VREFA-VREFB) varying from negative values up to 1200 mV, as shown in Figure 13.

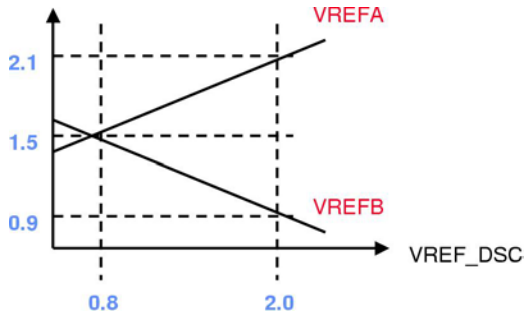

Figure 13. DTV features

The Figure 14 shows a simplified schematic of one DTV. First a constant common node is fixed to 1.5 volt. Then a DC current is flowing into the central branch through the two transistors and the three resistors. The two resistances on each side of the common node have then exactly the same voltage drop. This DC current is controlled by the voltage applied to the bottom resistor through VREF_DSC. The control of this DC current allows us to adjust the differential output voltage VREFA and VREFB.

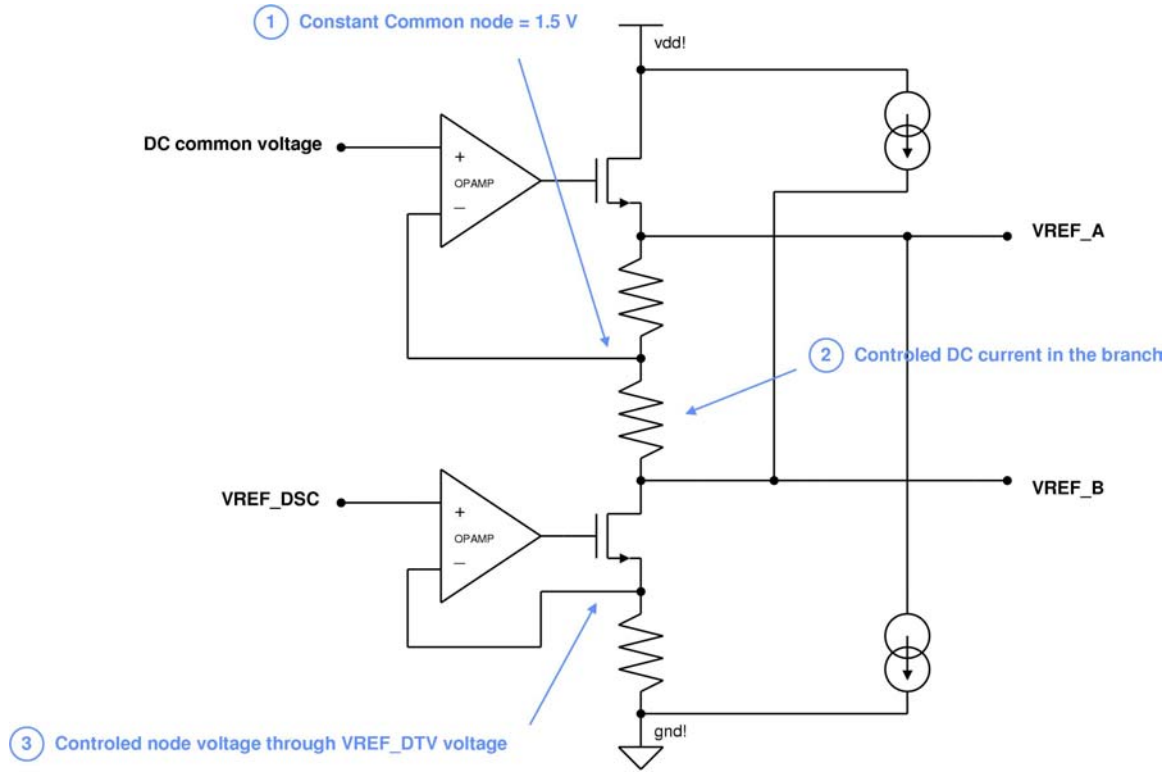

Figure 14. DTV simplified schematic

Inside the chip, there are 8 DTV's in total. There is the possibility to connect the DTV's in 2 different ways.

- Either, only one DTV (the top one) output is connected to the eight channels and set their threshold. In this case only the control signal VREF_DSC1 is used to set all the thresholds.
- Or each DTV output is connected to the corresponding channel. Then the eight VREF_DSC control signals are used.

The control signal "dtvSwitch" allow us to choose in between these to different configurations as drawn on Figure 15.

- "dtvSwitch" = 0 volt, means that only one DTV is used and
- "dtvSwitch" = 2.5 volt, means that the eight DTV's are used.

The pass-transistor logic (Figure 15) is used to make the connections in between the DTV's and the channels.

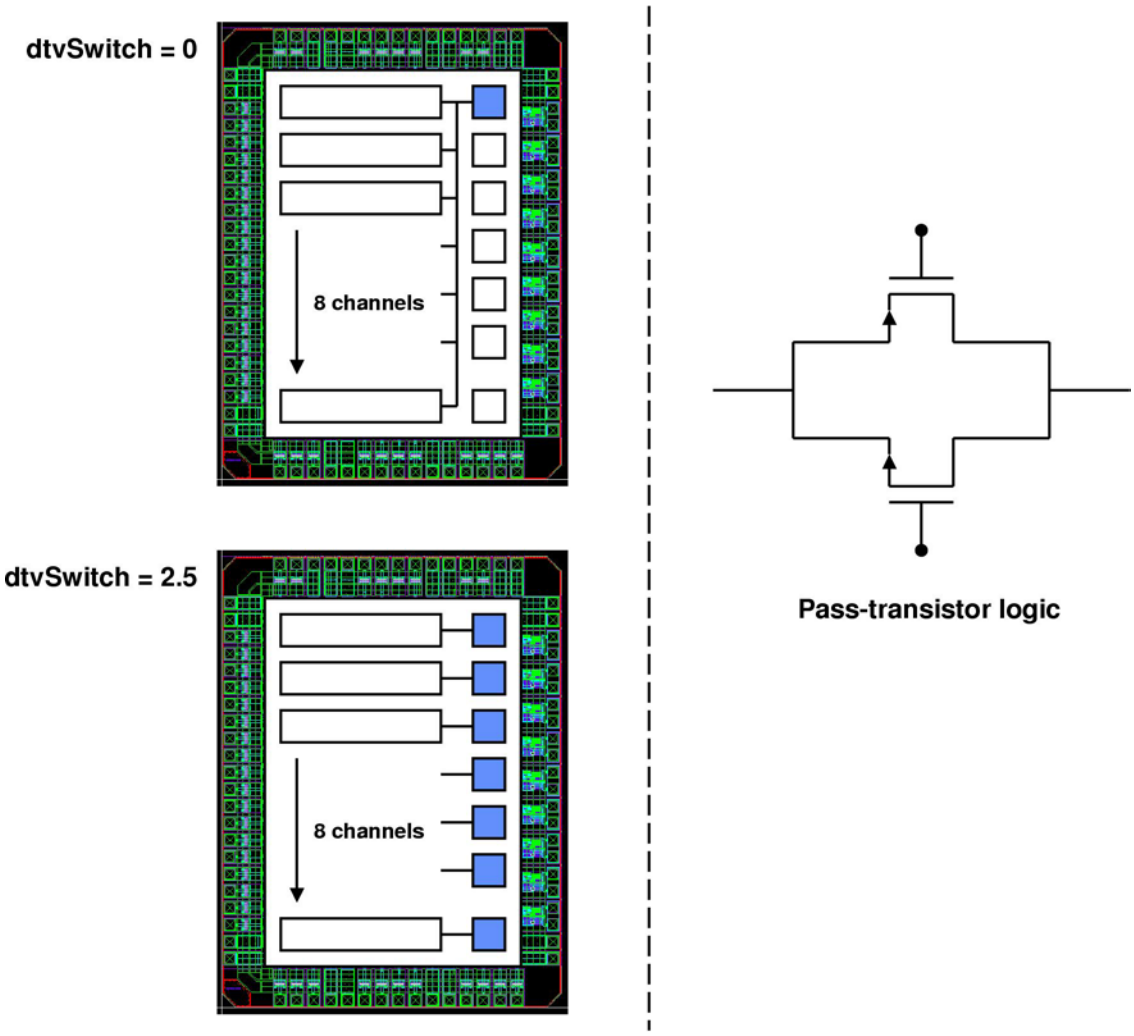

Figure 15. The control signal "dtvSwitch"

2.5 Internal pads

On the CARIOCA chip, there are internal pads that allow us to probe the nodes that are inside the signal processing chain, this means in between the blocks. This makes then easier the characterization of the different blocks. All the nodes in red in Figure 16 are connected to a simple source follower as analog buffer followed by the internal pad. All the channels have those internal nodes connected to such a pad.

The analog buffer prevents the capacitance load due to the picoprobe from affecting the internal signal shape. The picoprobe should be connected to a the scope coupling to 50 ohm DC, so that the 50 ohms allows the current flowing into the source follower and thus switch it on. When no picoprobe is probing the pad, the source follower is switched off and the internal node only sees a parasitic gate capacitance of 73fF.

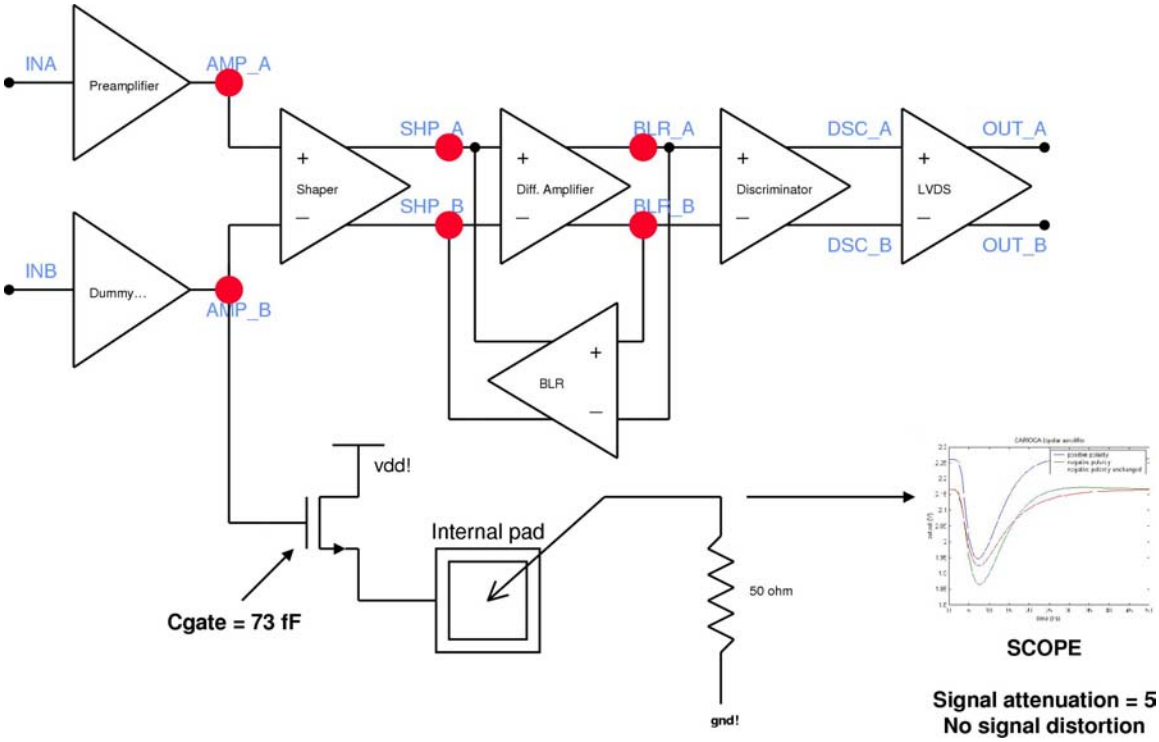

Figure 16. Internal pads and analog buffer

3 Ground and power supply lines distribution

On Carioca chip, both analog and digital signals are present. There are different ground and power supply lines, so that the digital signals do not disturb the analog blocks which are really sensitive.

The node gnd! Corresponds to the substrate. One can distinguish 5 different blocks with a specific ground and power supply lines :

- The preamplifier, connected to vdda! and gnd!
- The shaper, the differential amplifier and the BLR connected to vdd! and gnd!
- The discriminator splited in two parts :
    - Discriminator analog part connected to VPOS_DSC and gnd!
    - Discriminator digital part connected to VPOS2_DSC and VNEG2_DSC
- The LVDS driver connected to VPOS_LVDS and VNEG_LVDS.

The following Figure 17 shows the distribution of those ground and power supply lines on chip.

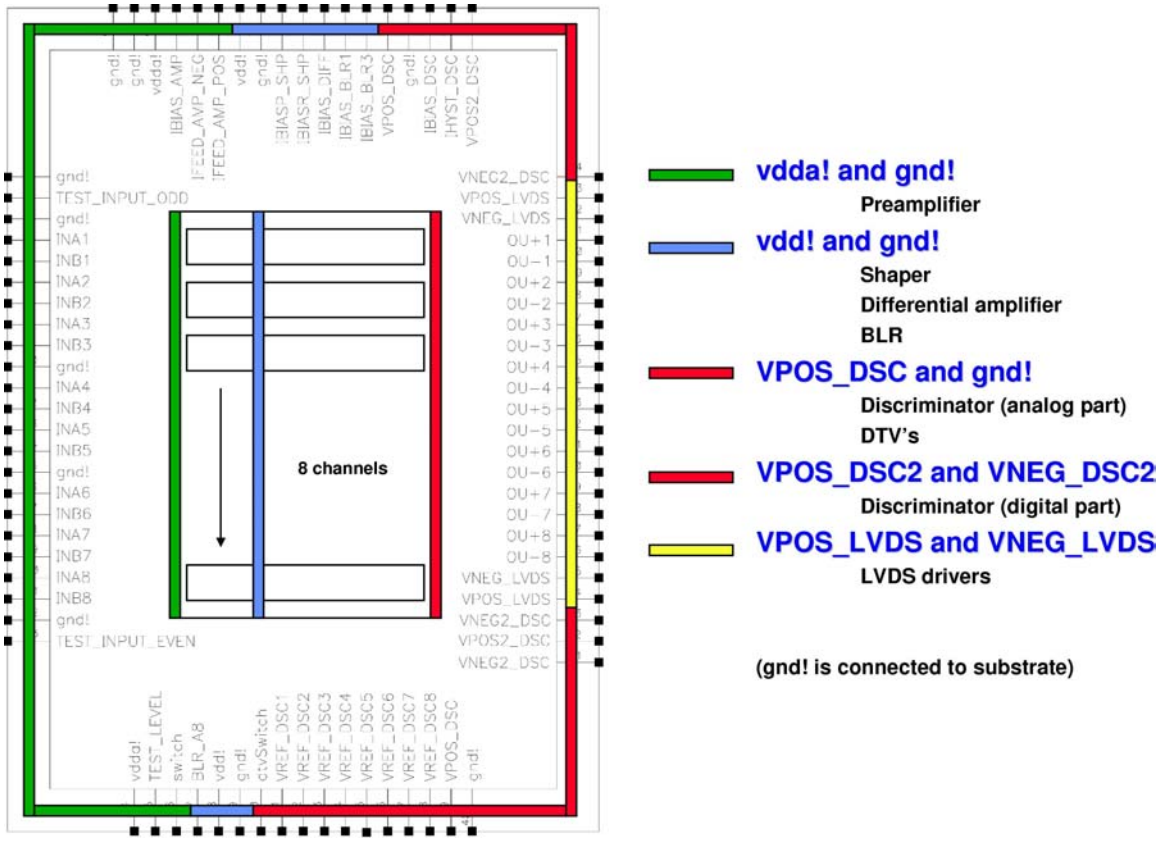

Figure 17. Ground and power supply lines distribution

4 ESD protections

During production and especially during manipulations and packaging phase, the chip has to be protected against Electrical Static Discharges (ESD).

The ESD strategy used for Carioca chip is the one described below in Figure 1. This is the common one used at CERN.

VPOS_LVDS power supply is used for VddCore.

The implementation of this ESD protection circuit adds some extra cells in the layout :

- The power clamps, and
- The diode chains.

Their positions will be described in the next sections.

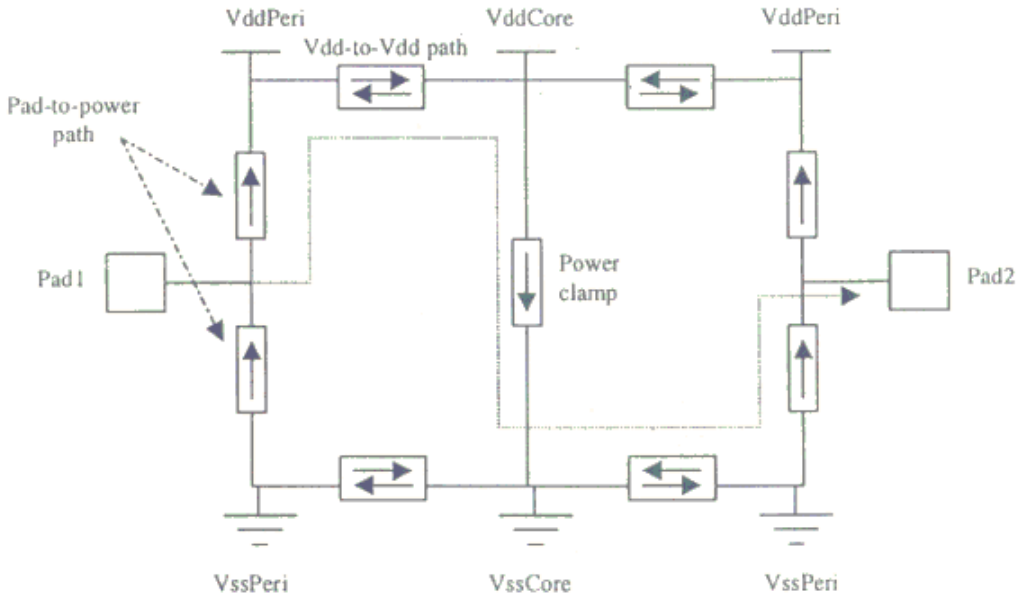

Figure 1: Schematic implementation of the current path ESD strategy[1].

Figure 18. ESD strategy

5 Chip pads

5.1 Pads description

The following Table 2 and Figure 19 describe the pads and shows their position on the chip.

Table 2. Pads description

Pad N°	Pad name	comment
1	gnd!	analog ground connected to substrate
2	TEST_INPUT_ODD	test input for odd channels
3	gnd!	analog ground connected to substrate
4	INA1	
5	INB1	
6	INA2	
7	INB2	
8	INA3	
9	INB3	
10	gnd!	analog ground connected to substrate
11	INA4	
12	INB4	
13	INA5	
14	INB5	
15	gnd!	analog ground connected to substrate
16	INA6	
17	INB6	
18	INA7	
19	INB7	
20	INA8	
21	INB8	
22	gnd!	analog ground connected to substrate
23	TEST_INPUT_EVEN	test input for even channels
24	vdda!	preamplifier power supply
25	TEST_LEVEL	sets the input charge when using the test inputs
26	switch	selects the preamplifier polarity
27	BLR_A8	BLR_A output of channel 8
28	vdd!	shaper, differential amplifier and BLR power supply
29	gnd!	analog ground connected to substrate
30	dtvSwitch	connects the discriminators either to the 1st DTV or to the 8 DTV's
31	VREF_DSC1	
32	VREF_DSC2	
33	VREF_DSC3	
34	VREF_DSC4	
35	VREF_DSC5	
36	VREF_DSC6	
37	VREF_DSC7	

38	VREF_DSC8	
39	VPOS_DSC	discriminator analog part power supply
40	gnd!	analog ground connected to substrate
41	VNEG2_DSC	discriminator digital part ground (not connected to substrate)
42	VPOS2_DSC	discriminator digital part power supply
43	VNEG2_DSC	discriminator digital part ground (not connected to substrate)
44	VPOS_LVDS	LVDS power supply
45	VNEG_LVDS	LVDS ground (not connected to substrate)
46	OU-8	
47	OU+8	
48	OU-7	
49	OU+7	
50	OU-6	
51	OU+6	
52	OU-5	
53	OU+5	
54	OU-4	
55	OU+4	
56	OU-3	
57	OU+3	
58	OU-2	
59	OU+2	
60	OU-1	
61	OU+1	
62	VNEG_LVDS	LVDS ground (not connected to substrate)
63	VPOS_LVDS	LVDS power supply
64	VNEG2_DSC	discriminator digital part ground (not connected to substrate)
65	VPOS2_DSC	discriminator digital part power supply
66	IHYST_DSC	
67	IBIAS_DSC	
68	gnd!	analog ground connected to substrate
69	VPOS_DSC	discriminator analog part power supply
70	IBIAS_BLR3	
71	IBIAS_BLR1	
72	IBIAS_DIFF	
73	IBIASR_SHP	
74	IBIASP_SHP	
75	gnd!	analog ground connected to substrate
76	vdd!	shaper, differential amplifier and BLR power supply
77	IFEED_AMP_POS	
78	IFEED_AMP_NEG	
79	IBIAS_AMP	
80	vdda!	preamplifier power supply
81	gnd!	analog ground connected to substrate
82	gnd!	analog ground connected to substrate

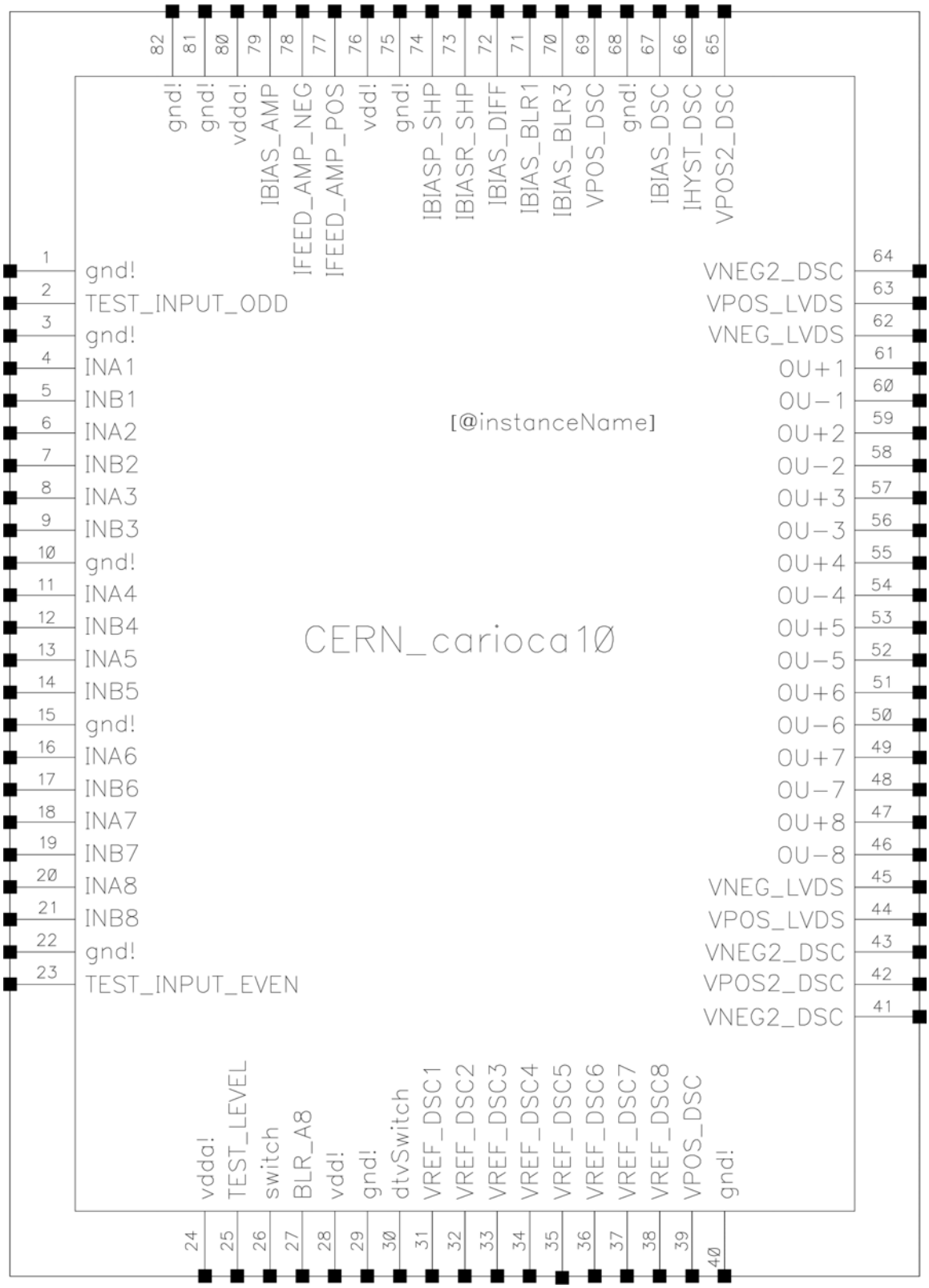

Figure 19. Chip pads

5.2 Pads for the bias

The following Table 3 gives for each bias pad the corresponding bias current and resistor value that has to be connected on the board (off chip).

Table 3. Pads for the bias

Pad name	Current (uA)	Resistor (Kohm)	chip1	chip2	Connected to…
IBIAS_AMP	150	was 9.1 and became 12	R7	R16	vdd!
IFEED_AMP_NEG	12	158	R25	R26	vdd!
IFEED_AMP_POS	18	100	R8	R17	gnd!
IBIASP_SHP	20	63	R10	R19	gnd!
IBIASR_SHP	40	39	R11	R20	vdd!
IBIAS_DIFF	55	30	R12	R21	gnd!
IBIAS_BLR1	50	35	R13	R22	gnd!
IBIAS_BLR3	50	35	R27	R28	gnd!
IBIAS_DSC	100	15	R14	R23	gnd!
IHYST_DSC	6	305	R15	R24	vdd!
switch					gnd! (negative polarity) vdd! (positive polarity)
dtvSwitch					gnd! (use 1 DTV) vdd! (use 8 DTV's)

6 Chip floorplanning and layout

The 6 following figures (Figure 20, Figure 21, Figure 22, Figure 23, Figure 24 and Figure 25) show the floorplanning of the whole chip and of the channel as well.

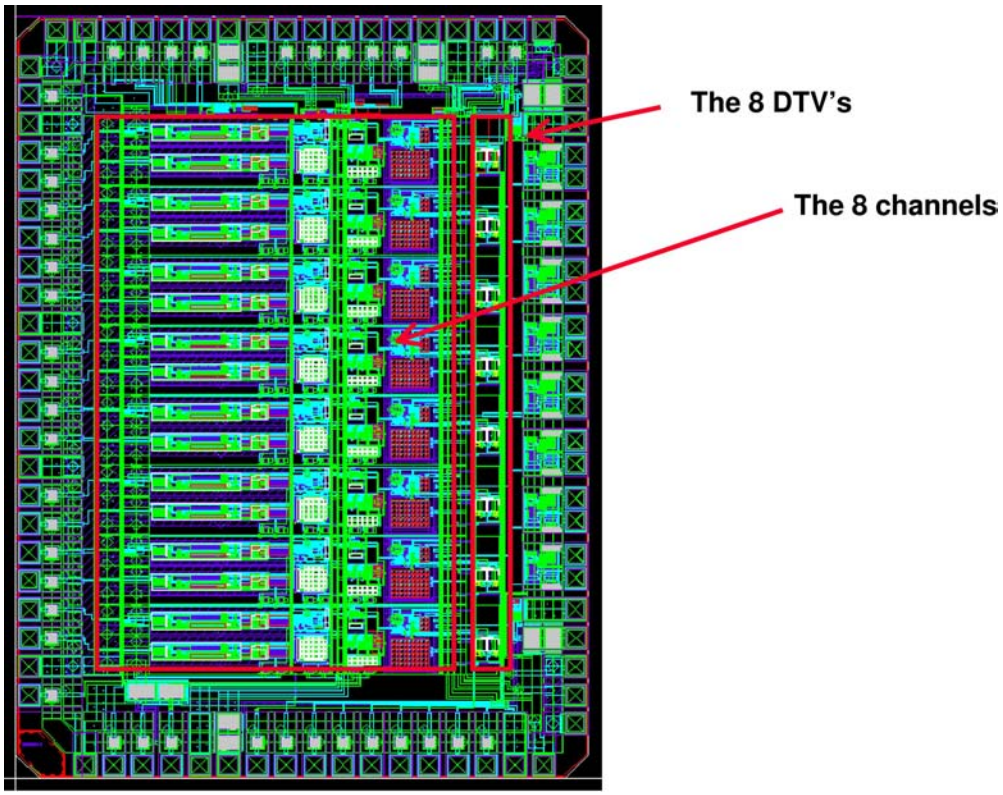

Figure 20. Layout : the 8 channels and the 8 DTV's

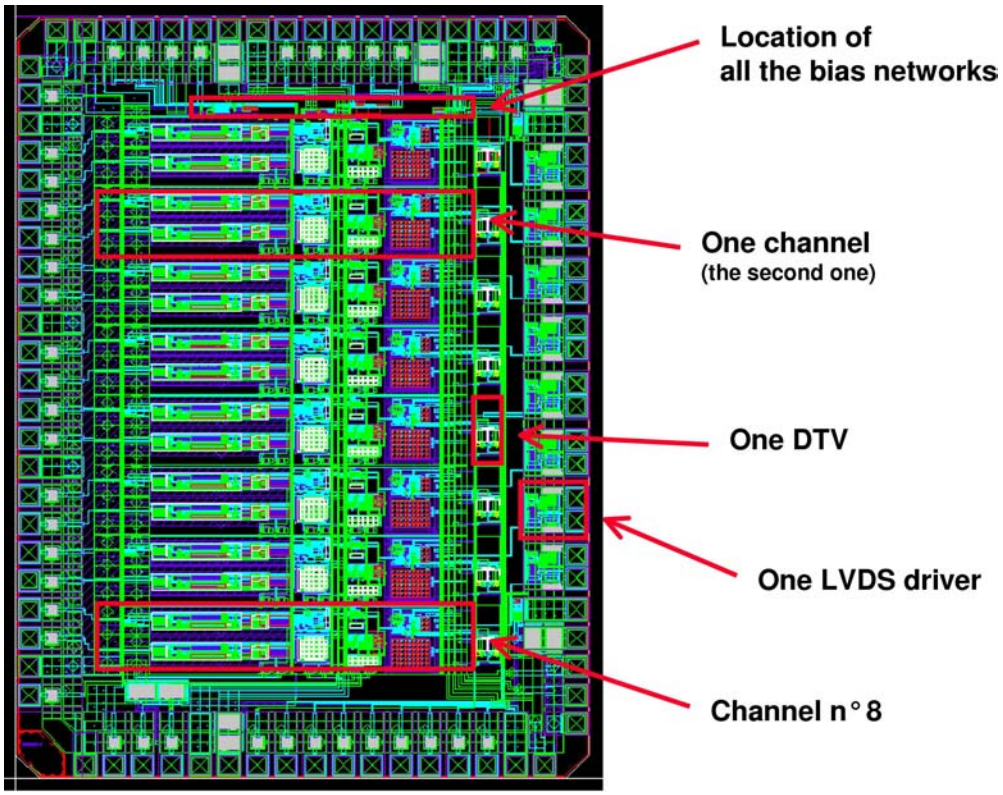

Figure 21. Layout : one channel, DTV, bias network

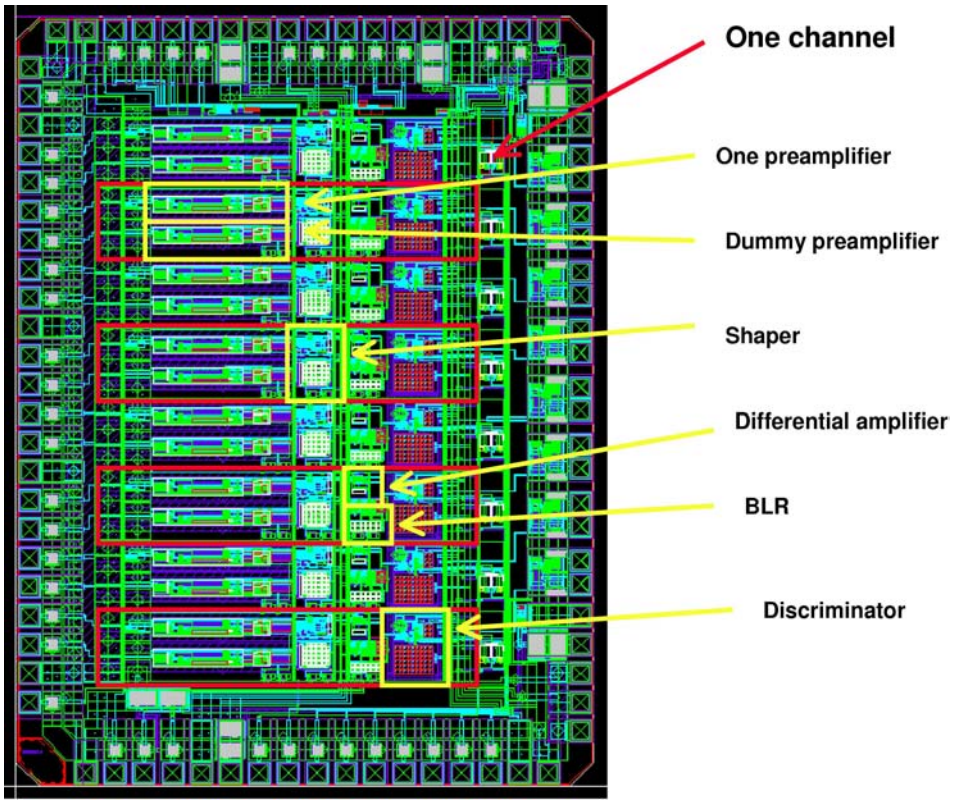

Figure 22. Layout : channel description

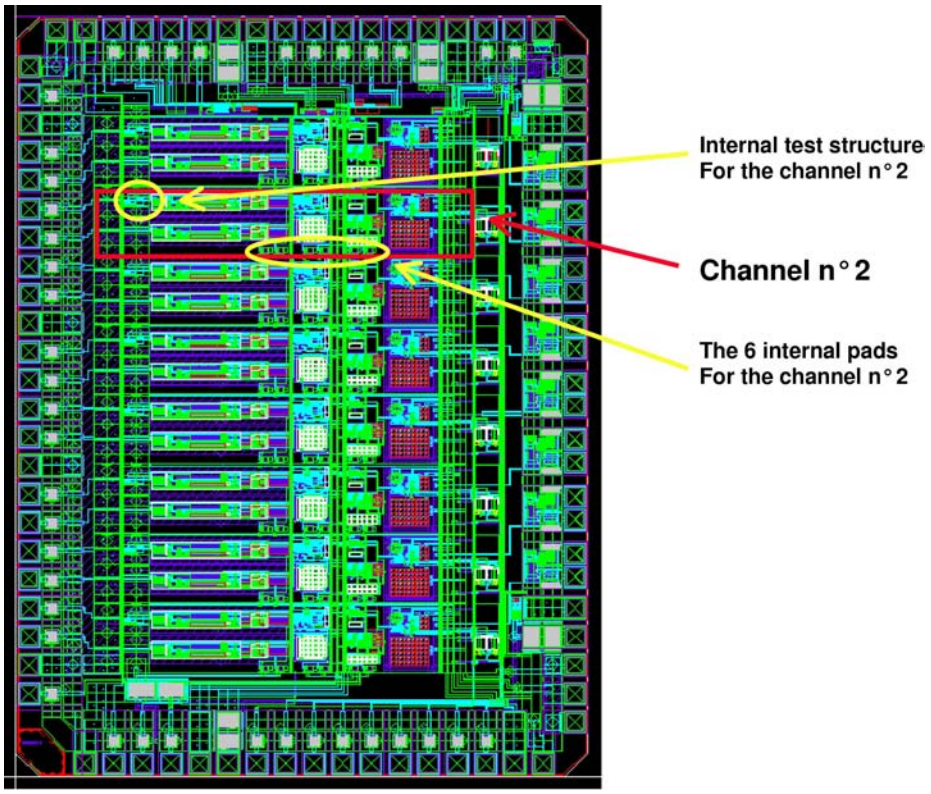

Figure 23. Layout : internals pads and internal test structure

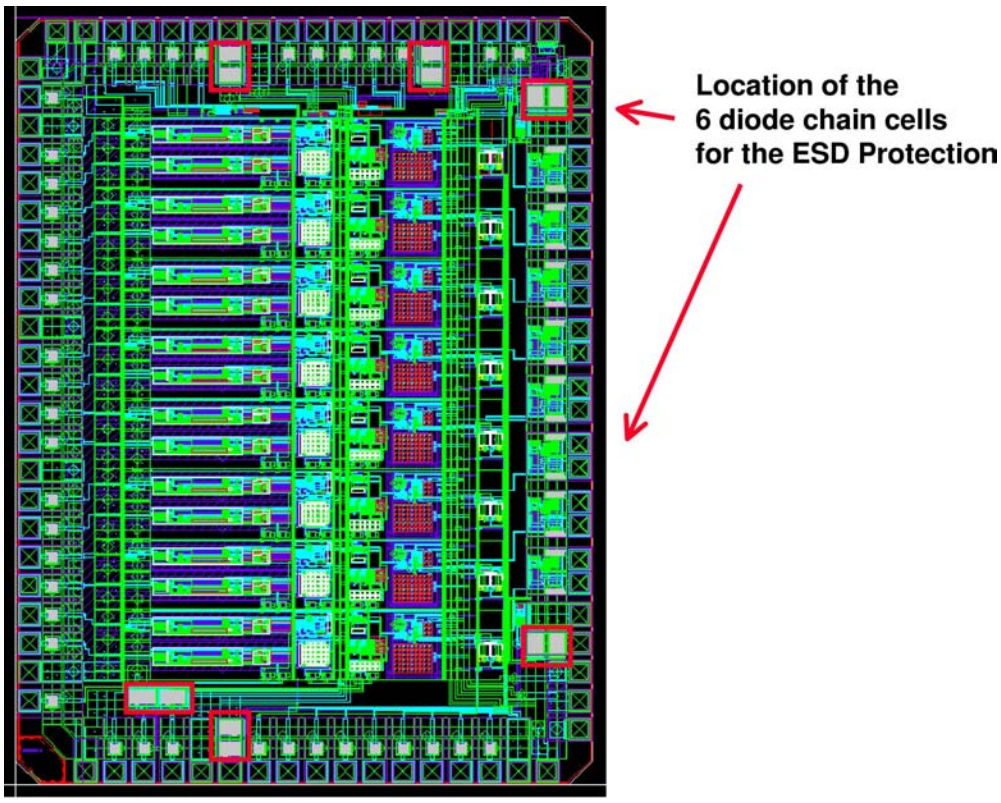

Figure 24. Layout : 6 diode chain cells

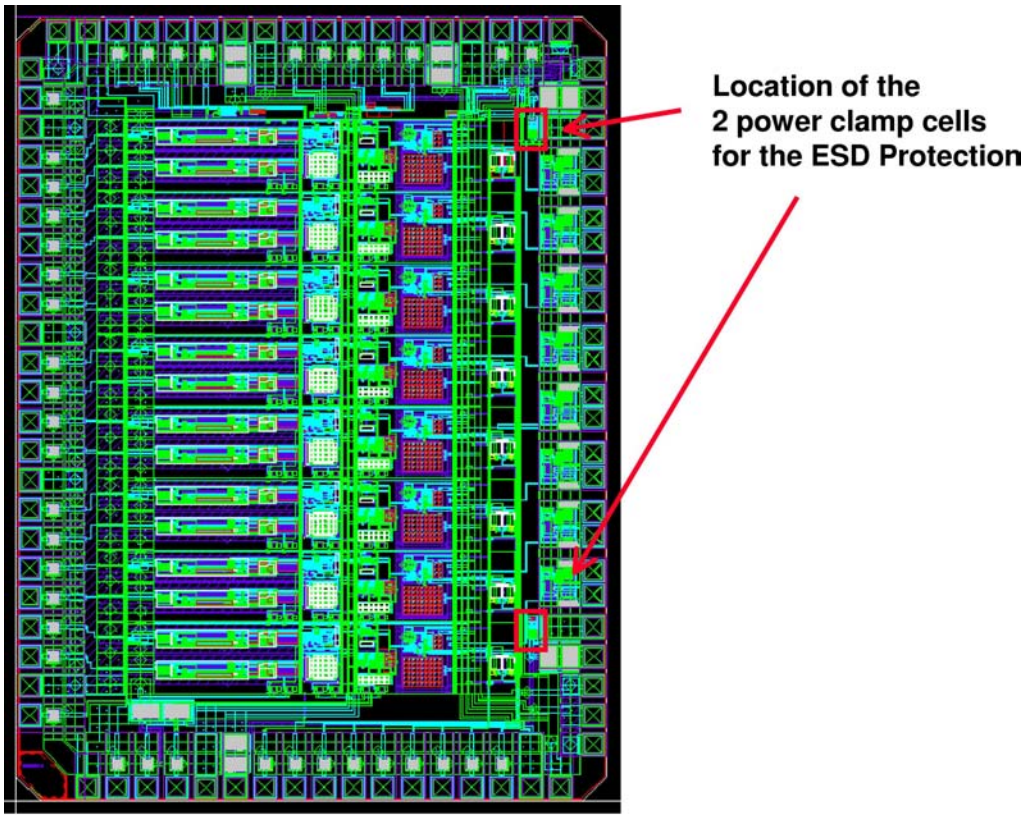

Figure 25. Layout : 2 power clamp cells

7 Libraries and files

7.1 The Libraries

There is one library for one submission. Here are the libraries with their corresponding prototype and submission MPW number (Table 4).

Table 4. CARIOCA libraries

Library name	Carioca prototype	Top Cell name	Submission	Designer	Design kit version
CARIOCA_2001_11	Carioca6	CERN_carioca_nasd CERN_carioca_pasd	MPW6	Danielle MORES	Version 1.0.1
CARIOCA_2002_04	Carioca7	CERN_carioca7_neg CERN_carioca7_pos	MPW7	Nicolas PELLOUX	Version 1.0.1
CARIOCA_2002_09	Carioca8	CERN_carioca8_bip CERN_carioca8_tst	MPW8	Nicolas PELLOUX	Version 1.0.1
CARIOCA_2003_02	Carioca9	CERN_carioca9	MPW10	Nicolas PELLOUX	Version 1.0.3
CARIOCA_2003_06	Carioca10	CERN_carioca10	MPW11	Nicolas PELLOUX	Version 1.0.3

All Those libraries above are completely independent with each other. But they refer anyway to some standard libraries that are mentioned on the next Table 5.

Table 5. Standard libraries used

Library name	Library path	Used for
analogLib		Schematic
cmos6sf25CoreLib	/vlsicad/micsoft/IBM_EP_kit_v1.0.3/designKits/cmos6sf25DesKit_v1.0.3/cmos6sf25/lib/cmos6sf25CoreLib	Schematic & layout
cmos6sf25PadLib	/vlsicad/micsoft/IBM_EP_kit_v1.0.3/designKits/cmos6sf25DesKit_v1.0.3/cmos6sf25/lib/cmos6sf25PadLib	Layout
RS_PCELLS_025	/homedir/szczygie/ibm102_test/RS_PCELLS_025	Layout

7.2 Libraries architecture

For each Carioca library, there are categories in order to find easily the cells. Among those categories, there are :

- "Chip" category where you can find the top cell view ("CERN_carioca10" in library "CARIOCA_2003_06" for instance) and
- "Simulation" category where you can find the simulation files :
  - "onechannel_simu" to simulate one channel and
  - "onechip_simu" to simulate the entire chip.

7.3 Where to find the library files

The following Table 6 gives the path where to get the Carioca libraries.

Table 6. Carioca library paths

Library name	Library path
CARIOCA_2001_11	/homedir/npelloux/IBM/CARIOCA_2001_11/
CARIOCA_2002_04	/homedir/npelloux/IBM/CARIOCA_2002_04/
CARIOCA_2002_09	/homedir/npelloux/IBM/CARIOCA_2002_09/

CARIOCA_2003_02	/homedir/npelloux/IBM/CARIOCA_2003_02/
CARIOCA_2003_06	/homedir/npelloux/IBM/CARIOCA_2003_06/

7.4 Where to find the submission files

The submission file are in the following folders :

- /homedir/npelloux/Submissions/MPW7_2002_04
- /homedir/npelloux/Submissions/MPW8_2002_09
- /homedir/npelloux/Submissions/MPW10_2003_02
- /homedir/npelloux/Submissions/MPW11_2003_06

In each of these folders, there are :

- CERN_CARIOCA<i>.GDS.gz : the concerning chip GDS file,
- CERN_CARIOCA<i>.TXT,
- CERN_CARIOCA<i>.<j>.GIF and
- Hercules_CERN_CARIOCA<i>.pdf : the waivers request file.

8 LVS matching

All the prototypes from carioca1 to carioca8 (library CARIOCA_2002_09) have been done using the design kit version 1.0.1. Then for the prototypes carioca9 and carioca10 (libraries CARIOCA_2003_02 and CARIOCA_2003_06), the version 1.0.3 is used.

The migration from version 1.0.1 to version 1.0.3 led to some problem for the LVS (Layout Versus Schematic) concerning the dummy devices.

For the same design,

- an LVS using the version 1.0.1 design kit leads to the output : " the net-lists match." and
- an LVS using the version 1.0.3 design kit leads to the output : "The net-lists match logically but have mismatched parameters."

These mismatched parameters concern only the dummy devices, especially the once that are in the shaper cell. And even when making the parameters correction so that the LVS matches for the chip, one gets once again an LVS that "matches logically but with mismatched parameters" for the channel cell.

Here is below a part of the LVS output for the whole chip, one have to live with.

```
…
The net-lists match logically but have mismatched parameters.

Probe files from /homedir/npelloux/IBM/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:
…
audit.out:
I /I165/I156/I45/M25
? WRONG LENGTH : 1e-05 instead of 2e-05 ;
I /I165/I156/I45/M21
? WRONG LENGTH : 1e-05 instead of 2e-05 ;
I /I165/I156/I45/M22
? WRONG LENGTH : 1e-05 instead of 2e-05 ;
I /I165/I156/I45/M17
? WRONG LENGTH : 1e-05 instead of 2e-05 ;
I /I165/I156/I45/M23
? WRONG LENGTH : 1e-05 instead of 2e-05 ;
…
I /I180/I156/M47
```

```
? WRONG LENGTH : 2.3e-05 instead of 0.0001 ; WRONG WIDTH : 1e-06
instead of 3e-06 ;
I /I112/I156/M50
? WRONG LENGTH : 2.3e-05 instead of 0.0001 ; WRONG WIDTH : 1e-06
instead of 3e-06 ;
…
I /I130/M1
? Combined device: WRONG LENGTH : 9.44394e-06 instead of 6.32456e-06 ;
WRONG WIDTH : 0.000230508 instead of 0.00015437 ;
…
I /I169/I203/M14
? Combined device: WRONG LENGTH : 9.44394e-06 instead of 6.32456e-06 ;
WRONG WIDTH : 0.000230508 instead of 0.00015437 ;
…
I /I112/I156/M45
? WRONG LENGTH : 0.0001 instead of 2.3e-05 ; WRONG WIDTH : 3e-06
instead of 1e-06 ;
I /I112/I156/M46
? WRONG LENGTH : 0.0001 instead of 2.3e-05 ; WRONG WIDTH : 3e-06
instead of 1e-06 ;


Probe files from /homedir/npelloux/IBM/LVS/layout
…
```